cadlab

Annual Report 1993

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Editors

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Cadlab Annual Report 1993

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PREFACE

Cadlab, the joint R&D institute of Paderborn University and Siemens Nixdorf Informationssysteme AG has been founded in 1985 with the goal of deeply integrating university research and industrial development in a joint centre of excellence. In this unique cooperation scientists, although hired from both sides, work together day by day under one roof, sharing common projects, solving common problems. The Bavarian Minister for European Affaires, Dr. Thomas Goppel called Cadlab "Ein in jeder Hinsicht herausragendes, zukunftsweisendes Beispiel (an example which under any aspects is exceptional and promising)".

Cadlab's objective is to advance the field of Computer Aided Concurrent Engineering (CACE) and to provide its partners with leading edge means and methods for solving complex engineering problems. During the report period a large number of publications have demonstrated the scientific success of Cadlab while its achievements in pre-competitive product development have been demonstrated by completing Cadlab's EMC-Workbench[1] to a state that is ready for a demanding and fast growing market. Due to its unique organisation and a consequent path from applied research to user oriented development, Cadlab can offer today one of the most advanced solutions worldwide in this area.

From the beginning Cadlab's work has been inspired by the vision of providing smoothly integrated environments to the user in order to optimise the overall engineering process instead of isolated tools. Consequently, in the past research and development on tools always included the aspect of building integrated tool sets or "workbenches". In recent years, due to the lack of basic integration services on the market, about half of Cadlab's efforts have been spent on the conceptualisation and development of a powerful integration system or "framework". This became a major contribution to SIFRAME, SNI's framework product, which emerged from the JESSI Common Frame (JCF) project, so that today an advanced framework is on the market. As a consequence Cadlab now concentrates on integration aspects not yet covered by SIFRAME. Important examples for such aspects are the federation of existing frameworks, the support of knowledge based engineering techniques and the information exchange via standardised formats. All these efforts are necessary steps towards the successful introduction of Computer Aided Concurrent Engineering into practical applications.

At the end of the report period, about 80 scientists and engineers plus about 90 student assistants and students preparing their master's thesis were employed in Cadlab. They are organised in three groups dealing with "Base Technology", "System Engineering Technology", and "Analog System Engineering". In addition there is a "Technical Management Group".

As the results achieved will be discussed in more detail within the following sections of this report, only some highlights shall be summarised here. So called "Federated Systems", i.e., the well organised cooperation of application centred frameworks will play an important role in the introduction of Concurrent Engineering into practice. This is due to the fact that in the various engineering domains to be combined in most cases local design environments already exist and cannot simply be replaced by a completely new environment. Cadlab developed a technology to solve this problem and will be able to offer this solution in the near future. Knowledge based techniques made considerable progress

[1] EMC: Electro-Magnetic Compatibility

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in the last years. As a consequence they enter more and more all areas of engineering. A successful CACE framework therefore has to support the integration of knowledge based tools. By means of its IFS[2] project, started during the report period, Cadlab will offer such support. The architecture follows the proposals of the IEEE working group P1252. Advanced user interfaces become more and more the key point of any computerised application. Based on its deep knowledge in this field Cadlab started a new project in this area with the goal to design and implement an advanced, platform independent editing system. First results are operational and have been used to build applications. Concurrent Engineering means integrated engineering with heterogeneous engineering domains. While the user prefers to stay at the modelling environment he is familiar with, internally a unified modelling method has to be provided. A solution to this problem is an essential pre-requirement for successfully introducing CACE. During the report period at Cadlab a very promising approach, based on enhanced Predicate/Transition nets has been developed. The communication of data to the outside world is increasingly based on STEP protocols. To support this trend a STEP/EXPRESS workbench has been designed at Cadlab. It is highly generator-oriented and therefore extremely flexible. A first release has been finished during the report period. Cadlab's most complex software system completed in the report period is the EMC-workbench. It is one of the leading design environments worldwide to support the design of electronic systems under EMC constraints. The successful use of this software within various departments of SNI demonstrated its quality and fundamental importance. Therefore it is not surprising that there is a remarkable external market pull for this software.

The application driven research and development of Cadlab makes it necessary to participate in externally driven projects. During the report period Cadlab participated in an ambitious project on defining an innovative CAI/CACE[3] concept for SNI's System Unit "Midrange". This type of project is intended to become a standard Cadlab activity.

From its beginning Cadlab has been participating in large nationally and European funded projects. In 1993 two of them have been successfully finished: EMC-Design, funded by BMFT[4], and ECIP II, funded by the CEU[5]. A couple of additional projects have been continued or newly started during the report period. This demonstrates Cadlab's reputation in the scientific and technical community.

Cadlab's standardisation efforts have been concentrated on active participation in various international bodies. Areas of Cadlab's standardisation contributions include VHDL, EXPRESS, Inter Tool Communication, Framework Architecture, Data Modelling, Simulation Backplanes, Object Oriented Databases, Engineering of Computer-based Systems.

Cadlab's international scientific reputation is reflected by the large number of publications. Cadlab employees have presented papers on most major international conferences on topics related to Cadlab's focus of research. In addition, Cadlab members have been active in organisational bodies of such conferences. Among the many outstanding scientific achievements, the international first price for graphical data processing received by R. Zhao for his work on pen-based computing deserves special recognition.

1993 was a year that demonstrated the intent and ability of Cadlab to anticipate upcoming demands and interests of Cadlab's constituting partners as well as trends and

[2] IFS: Intelligent Framework Services
[3] CAI: Computer Aided Industry
[4] BMFT: Bundesministerium für Forschung und Technologie
[5] CEU: Commission of the European Union

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developments in the international research and user community. By concentrating on leading edge pre-competitive areas the workforce could be focussed on future-oriented goals. On the other hand, Cadlab has kept its proven main principles: tight integration of academic research and industrial development and focus on application oriented research and development topics.

The following annual report gives an overview of Cadlab's activities and achievements in 1993. Part I of the report details Cadlab's objectives, describes Cadlab's organisational structure and gives a general overview of the progress made. Part II contains technical details from the project groups. Part III provides supplementary information on publications, funded projects, and cooperations.

F.J. Rammig and B. Steinmüller
Cadlab Executive Board
Paderborn, June 1994

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Part I
Overview

1 Goals and Objectives

1.1 Mission

Cadlab, the joint research and development institute between Paderborn University and Siemens Nixdorf Informationssysteme AG, SNI, has been founded in 1985 with the *mission* to deeply integrate university research and industrial development in a *"joint centre of excellence"*, for the synergetic benefit of both partners.

This cooperative approach yields new possibilities for academia, namely to open-up and further new application-oriented research areas, while at the same time industry gains a sound, knowledgeable basis for developing leading-edge means and methods for mastering real-life, complex engineering problems. Last, but not least, this approach yields a very stimulating working atmosphere and a fruitful ground for the development of highly qualified application-oriented engineers and scientists.

1.2 Guiding Theme and Central Topics

Cadlab's R&D work in the nineties is guided by the overall theme *"Computer Aided Concurrent Engineering (CACE)"*.

Here, *"Concurrent Engineering (CE)"* stands for a systematic approach to the engineering of products, characterised by the early, concurrent consideration of all product aspects that are relevant through its further life cycle.

The key objectives of CE are

- lead time reduction
- improvement of product and environmental quality
- improvement of competitiveness

Computer Aid (CA) is seen as a pre-condition for efficiently implementing CE and for mastering CE complexity. Due to its practical importance and its academic potential, "CACE" is of high strategic interest for both partners within Cadlab.

Under this guiding theme, Cadlab focusses on the following areas of work:

- Integrated System Engineering
- Analog System Engineering
- Base Technology (CACE-Infrastructure)

These areas have been described as part of a new work programme in 1992, which has been formally issued by the Cadlab Advisory Board in the beginning of 1993.

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1.3 Results and Services

Cadlab's material results are given by

- Research and development reports in the area of CACE
- Publications and PhD theses
- Software prototypes
- Software components with industrial quality standard

Cadlab's services include

- Education and training of students and employees in application-oriented projects ("training-on-the-job")
- Coordination and support of complex R&D projects
- Execution of user projects
- User consultancy
- Transfer of know-how and software

1.4 Objectives of the Report Period

While a new CACE work programme and new organisational structures have been defined in the previous report period, a major objective of the last report period was the initialisation of the work programme in the new field of base technology and integrated system engineering.

The major goal consisted in the evaluation of the relevant problem spaces, collection of user requirements and development of first prototypes and models. Moreover, a key objective was the effective take-up of leading-edge research results previously achieved by Cadlab in the areas of advanced user-interfaces, system- and data-modelling (cf. annual report 1992). In line with the idea of concurrent engineering (as applied to our own tasks) a major goal was the early assessment of potential markets and user requirements by means of close user interaction. Consequently an engineering process had to be set-up, which - while enabling adequate milestone-based process-control - was flexible enough to allow fast response to new inputs.

As for the field of "Analog System Engineering" a key goal was the industrialisation of the highly advanced computer-based workbench for Electromagnetic Compatibility EMC and its application within SNI. In particular, all necessary steps for technology transfer into a commercial context were to be taken. At the same time, new R&D areas in the analog system engineering context were to be prospected.

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2 Organization

2.1 Overview

Cadlab is a joint venture between Paderborn University and Siemens-Nixdorf Informationssysteme AG (SNI). The financial support comes from SNI and the federal state of Nordrhein-Westfalen to about equal amounts. Additional funding is provided by the CEU and the BMFT by financing a number of research projects.

The basis of the cooperation is a contract between the two partners. The cooperation is open to further partners from academia or industry. The management of Cadlab is carried out by an executive board of two directors, one from the university and one from SNI. The executive board of directors is advised by an advisory board in technical and organisational matters (cf. Figure 1).

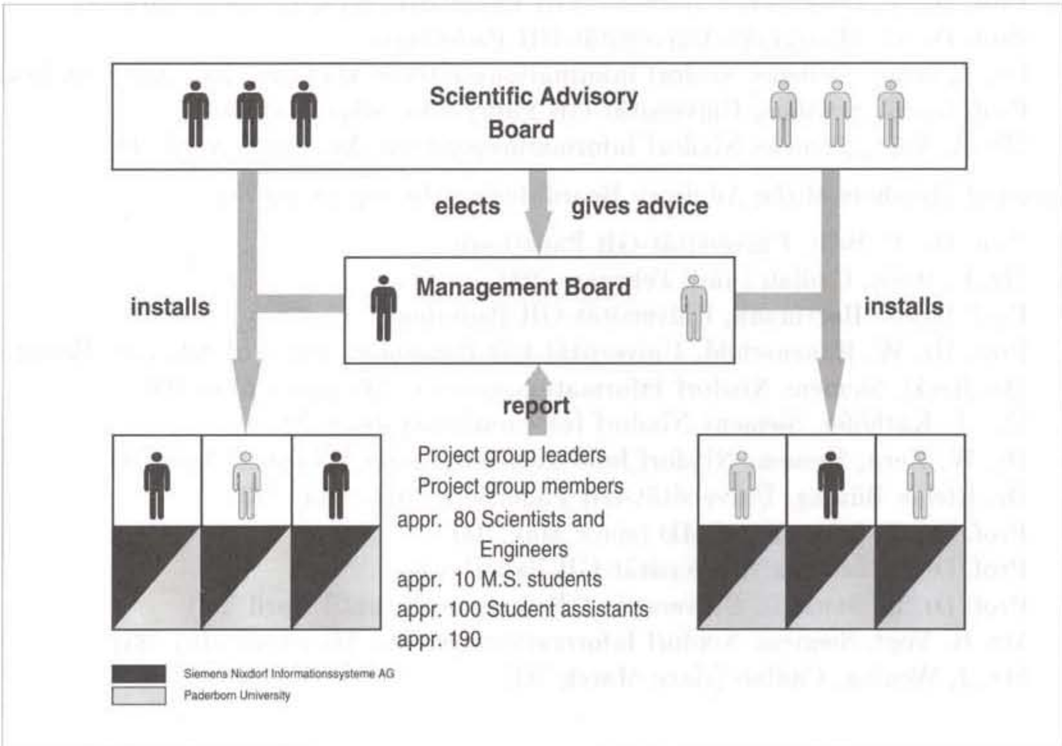

Figure 1: Cadlab, Principal Organisational Structure

The joint scientific and technical work is performed in project groups which are headed by project group leaders (see Fig. 1). Depending on specific needs these principle entities can be combined into larger or further sub-structured into smaller working groups. In particular, the project groups in the domains "Framework/Base Technology", "System Engineering Technology" and "Analog System Engineering" have been combined to form corresponding super project groups, which take care of the special coordination needs in these domains.

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2.2 Advisory Board Members

Executive Board of Directors during the report period:

Prof. Dr. F.J. Rammig, Cadlab (Universität-GH Paderborn)
Dr. B. Steinmüller, Cadlab (Siemens Nixdorf Informationssysteme AG)

Chairman of the Advisory Board:

Prof. Dr. W. Hauenschild, Universität-GH Paderborn

Members of the Advisory Board during the report period:

Mr. Heckl, Siemens Nixdorf Informationssysteme AG (until April '93)
Mr. Held, Siemens Nixdorf Informationssysteme AG (since May '93)
Prof. Dr. U. Kastens, Universität-GH Paderborn
Dr. W. Kern, Siemens Nixdorf Informationssysteme AG (since May '93)
Prof. Dr. T. Lengauer, Universität-GH Paderborn, (GMD) (until April '93)
Prof. Dr. G. Mrozynski, Universität-GH Paderborn
Dr. T. Sauer, Siemens Nixdorf Informationssysteme AG (vice chair Advisory Board)
Prof. Dr. G. Szwillus, Universität-GH Paderborn (since May '93)
Mr. H. Vogt, Siemens Nixdorf Informationssysteme AG (until April '93)

Associated Members of the Advisory Board during the report period:

Prof. Dr. F. Belli, Universität-GH Paderborn
Mr. F. Buijs, Cadlab (until February '93)
Prof. Dr. G. Hartmann, Universität-GH Paderborn
Prof. Dr. W. Hauenschild, Universität-GH Paderborn (chair of Advisory Board)
Mr. Heckl, Siemens Nixdorf Informationssysteme AG (since May '93)
Mr. T. Kathöfer, Siemens Nixdorf Informationssysteme AG
Dr. W. Kern, Siemens Nixdorf Informationssysteme AG (until April '93)
Dr. Kleine Büning, Universität-GH Paderborn (since May '93)
Prof. Dr. T. Lengauer, GMD (since May '93)
Prof. Dr. B. Monien, Universität-GH Paderborn
Prof. Dr. G. Szwillus, Universität-GH Paderborn (until April '93)
Mr. H. Vogt, Siemens Nixdorf Informationssysteme AG (since May '93)
Mr. J. Wening, Cadlab (since March '93)

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3 Summary of Progress

Work in the report period was driven by the mission and objectives summarised in chapter 1 above. The activities in the domain of Information Technology were largely executed in the two main groups on CACE "Base Technology (BT)" and "System Engineering Technology (SET)", while the Cadlab activities in the domain of Electrical Engineering were concentrated in the main group "Analog Systems Engineering (ASE)".

In CACE Base Technology (BT) a new research and development programme has been initialised (cf. chapter 4). This programme is directed at further extending the powerful capabilities of the JESSI Common Framework JCF/SIFRAME with new CACE services. These services are offered in a modular, portable way. Besides providing functional extensions to JCF/SIFRAME, the new CACE components can also be used outside JCF/SIFRAME. In particular, powerful facilities are offered, which support the integration and coupling between other external frameworks and CAx-Systems.

In the report period, the problem space of CACE/BT was investigated and projects on "Data Base Federation, DBF", "Advanced Editing Systems, AES", and "Intelligent Framework Services, IFS" were started. Thereby the DBF project not only treats the imminent problem of coupling heterogeneous, distributed databases, but also offers services and strategies for stepwise transforming heterogeneous systems into uniform ones by means of migration. In all projects prototypes were built and discussed with potential industrial users. These prototypes included to a large extent the results of research work performed in previous report periods. This way, a flying start could be achieved. Parallel to these development oriented activities, further applied research work was carried out in the areas mentioned as well as in "design transaction management" and "object oriented integration".

As far as the area of "System Engineering Technology SET" (see chapter 5) is concerned, the main target is the development of integrated generic environments for system development and control. In the context of CACE this includes both the "engineering of concurrent systems" and the "concurrent engineering of systems".

Similar to BT, a key objective in SET was the initialisation of a new R&D programme. This programme includes the exploitation of previous research results as well as the exploration of relatively new fields with a high application potential. As far as exploitation is concerned, work focussed on the industrialisation of the experience gained in the field of STEP/EXPRESS. Here, an integrated tool environment or "workbench" is under construction, which supports graphical system modelling in line with international standards. A key component of this workbench - the advanced syntax and semantic checker ICE - has already been made publicly available free of charge via the ftp server of Paderborn University. Moreover, a base version of the EXPRESS-G editor "EXPREME" for the fast, graphical design of EXPRESS models has been implemented.

Research in SET focussed on system modelling for the concurrent design of heterogeneous systems. Here a key assumption is that a CACE environment has to support different external views and models optimised for the corresponding application domain, while at the same time a common kernel model is needed to support communication between these different views. Extended timed Predicate/Transition nets were chosen as the basis for this kernel model. Research studies underlined the strengths of this approach. In particular, it could be shown how this kernel model enables the integration of digital and

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analog/physical aspects as for example required for the design of mechatronics systems.

The activities in the domain of "Analog System Engineering" (see chapter 6) are focussed on the development of tools and methods for the design of electronic circuits and systems under EMC-constraints. EMC stands for "Electro Magnetic Compatibility" and addresses a problem area, which has become ever more critical with the adventure of high speed electronic systems. Effective solutions in this problem area necessitate the anticipation of EMC-effects early in the design process by means of sophisticated computer aided design and analysis techniques, i.e., by adopting a CACE-approach.

In the given report period the integrated EMC-tools and techniques developed in Cadlab over the last number of years have been successfully industrialised and are now available as a product quality "EMC workbench" from Cadlab's partner SNI. Besides, library components, macro models and interfaces to different commercial CAD systems have been set-up and integrated into the workbench. The workbench is characterised by a high user orientation and practice-proveness, which has been achieved by developing the workbench in close conjunction with EMC-consultancy in SNI computer manufacturing plants. During the last report period all new SNI SINIX-computer designs have been successfully analysed and refined by Cadlab engineers using the Cadlab EMC-technology. Thus, the EMC-workbench has been successfully used and beta-tested in a highly demanding, practical production environment.

Apart from the development of new components, the extension of the EMC-CACE approach to new application domains has been undertaken. A generic design process model has been constructed and implemented. This model now can be customised to optimally suite particular application requirements. Special consideration has been given to the domain of micro-systems, which currently is positioning itself as one of the promising key technologies in Europe's industrial future.

Efficient support for the ongoing R&D work was provided by the Cadlab "Technical Management Group, TMG" and the "Computing Centre, CC" (cf. chapter 7). Thereby TMG also provided internal and external CACE-consultancy. This way know-how transfer was effectively supported, while at the same time new ideas and requirements for Cadlab's future work were collected. Last, but not least, TMG was active in project support and acquisition for Cadlab as well as for Cadlab's partners. The Cadlab Computing Centre, CC, efficiently maintained a complex network environment with more than one hundred workstations and twenty PCs. CC also continued to support a closely related SNI unit, which formerly belonged to Cadlab.

Most of Cadlab's work was carried out in the context of collaborative projects (see chapter 9). Concerning nationally funded collaborations, Cadlab has participated in eight BMFT projects, two of them executed in the frame of the European JESSI programme. Thereby, the large European EMC project JESSI AC-5 is also led by Cadlab. Three more projects are funded by ESPRIT, one of them being the JESSI project AC-1 on frameworks, which Cadlab has successfully managed during the last reporting periods.

Publications and dissemination of technical/scientific results again played a major role also in this report period (see chapters 8–10). A number of master theses were completed under the supervision of Cadlab employees. Among the many outstanding scientific achievements, the international first price for graphical data processing received by R. Zhao for his work on pen-based computing deserves special recognition.

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Part II

Project Group Reports

4 Base Technology

4.1 Baseline

The project group "Base Technology" was formed in October 1992 with the mission to investigate infrastructures needed for CACE and to provide basic services for building CACE environments. These services should be offered as flexible software building blocks, such as to be useful in a wide range of practical environments. In particular, smooth inter-operability with JCF/SIFRAME^{TM}[6] is planned.

Among the CACE-services to be built, the following ones should be emphasised in the beginning:

- Innovative interaction and presentation services
- Federation services for heterogeneous, distributed systems
- Framework services for knowledge-based techniques

Accordingly, the tasks of base technology are executed in three subgroups: UI (User Interface), DI (Data-oriented Integration), CI (Control-oriented Integration). The baselines for these groups and the work performed during the report period are detailed below.

4.1.1 User Interface, UI

At the beginning of 1993, two research prototypes were completed as the results of two PhD theses within this project group. The first one is called Handi (Hand-sketch-based Diagram Editing), the name of the second one is Edis (Editor Description and Implementation System).

Edis provides a concept to separate dialogue control of graphical editors from presentation. Instead of call-backs and event-handlers, non-blocking input requests are used to couple presentation and dialogue control. This allows an abstract description of the end-user's commands, without loosing features like direct manipulation and semantical feedbacks.

Handi is a framework for building hand-sketch-based diagram editors and has been designed for reducing the efforts required by building gesture-based diagram editors. It provides concepts and mechanisms for on-line recognising hand-sketches and for specifying gestures as editing commands. The basic idea of Handi is to encapsulate common characteristics of hand-sketch-based diagram editors into classes by using an object-oriented methodology. Handi specialises basic abstractions of general editor frameworks for directly supporting common features of diagram editors.

[6] Siemens Nixdorf Informationssysteme AG, SIFRAME Product Sheet, 1993.

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In order to transfer these practically relevant research results into industrial re-usable products, the project AES (Advanced Editing Systems) was initiated. One of the most important goals of the AES project has been to transfer the research results into products. Furthermore, there is much internal and external need to support the development of graphical editors. Under these considerations, the project has two aspects: The first aspect is to transfer the research results into a product, in form of an editor framework; the second one is to develop application-specific graphical editors.

4.1.2 Data-oriented Integration, DI

Within Cadlab, the project group "Data-oriented Integration, DI" covers the field of object-oriented database technology and its applications. In former years work in this field was focussed on research and development of components for a single object-oriented database system. For example, development of components for JCF/SIFRAME data handling system was supported.

Investigating data handling facilities within CACE environments has shown, that new requirements have to be fulfilled. In particular, the user and system communities must have autonomous access as well as uniform global access to already existing and new data repositories. Here, data repositories are represented by file systems and database systems of different technologies.

Due to these requirements focus of the project group DI is the development of "Database Federation Services, DBF". The aim of this work is the federation of homogeneous resp. heterogeneous, autonomous databases. Here, federation and coupling of object-oriented database systems together with database systems based on the relational model or the entity-relationship-model is of interest. The "Database Federation Services" offer a solution in form of a logical, homogeneous software layer on top of the homogeneous resp. heterogeneous databases to be federated. This software layer can be used as a "stand-alone" component as well as an integrated component of JCF/SIFRAME.

To enable the tasks of the DBF project several fundamental components from the field of database technology have to be developed. For example, graphical editors for defining database schemas, data dictionaries for storing and retrieving information about the federated database systems, and database interfaces for defining, manipulating and querying data within the federated system were developed. Database interfaces need to be developed under consideration of current resp. upcoming standards in database technology, for example SQL-2 and Object Database Management Group (ODMG).

4.1.3 Control-oriented Integration, CI

In the past years considerable progress has been made in research and development of knowledge based systems as well as knowledge base infrastructure, which is called "shell" in this context. Nevertheless, these systems have not been as successful as expected some years ago. One of the identified reasons is the lack of integration facilities of these usually stand-alone systems. Therefore, a key requirement is to provide a comprehensive methodology for the development of knowledge based systems, and to integrate and maintain intelligent services in JCF, which utilise these techniques.

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To enable this task the project *Intelligent Framework Services* (IFS) was started in March 1993. The goal of this project is to provide an infrastructure to support the development of tools which use declarative knowledge to perform intelligent behaviour, and which can be deeply integrated within a CACE environment. The second requirement posed on IFS is to follow the toolbox approach, thus permitting to use only those modules of knowledge based services which are required to fulfil the task of a certain tool.

Knowledge representation is one of the central design problems. For the hybrid knowledge description language HyKL therefore a combination of frame-based representation mechanism with rule-based reasoning needs to be employed.

For the development of the frame-part of HyKL, a proposed IEEE standard is used as a base. This *Standard for a Frame-Based Knowledge Representation* is developed by the IEEE working group P1252.

4.2 Work During the Report Period

4.2.1 User Interface, UI

Within the report period, the project group "User Interface" changed the focus from research to development of graphical software systems. The project AES (Advanced Editing Systems) was initiated, to transfer the results of the two research projects Handi and Edis into an industrial re-usable product. The current working title of this project is EOS (Editor operating system). EOS is an editor framework, which can be used to easily implement highly interactive applications, in particular graphical editors. In order to evaluate the concepts of EOS in practice, the concurrent development of two EOS-based editors has been supported and supervised. The first editor is an EXPRESS-G editor called EXPREME. The second editor is called SCALOR and is similar to an PCB layout editor with additional features required by the EMC Workbench.

Besides the AES project, support for the desktop application of SIFRAME 3.0 has been an important activity.

4.2.1.1 Project Advanced Editing Systems (AES)

The project AES was initiated in February 1993 and was managed by following the SNI Process Technology with Cadlab adaptations. Within the SNI Process Technology, a project has to pass several project master process steps. Within the report period, the AES project completed the first master step, the "Problem Analysis", the second master step, the "Product Definition", was started and is in progress at the moment.

In the "Statement of Problem" which is the first phase of the problem analysis, the problems were classified into two basic classes. One are the problems of the end-user and the other are the problems of the editor programmer. Furthermore, the customers of this project and the relationships between the domain of the general user interface and the domain of graphical editors are considered.

In the "Initial Situation Analysis", which is the second phase of the problem analysis, the current situations were analysed. This includes the analysis of user's problems, the general problems of user interface programming, and the status of current editor projects. Furthermore we considered the platform constraints and in-house technology basis. An

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evaluation of existing editor frameworks and user interface toolkits were performed for making decisions about platform and base software. One of the important aspects is the use of pen-based computing in conceptual design and in the computer supported cooperative work. A NCR Notepad computer was procured for the evaluation.

In the "Problem Space Specification", which is the third phase of the problem analysis, a conceptual model of the solution environment was worked out. In our model, the end-user's environment was described and the programmer's environment was considered with supporting tools and run time structures of generated editors. Furthermore the module structure of the editor framework was designed as shown in Figure 2.

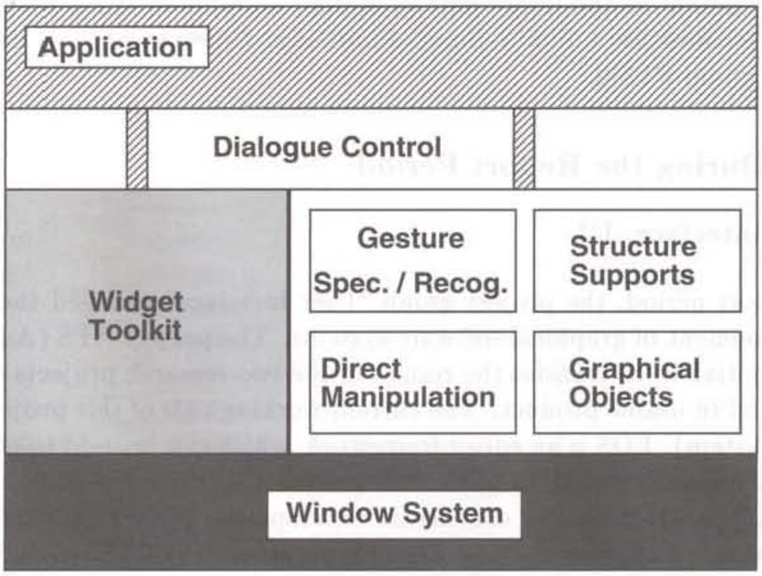

Figure 2: Module Structure of the Editor Framework

4.2.1.2 EOS

Within the report period, the user interface group developed a prototype editor framework, called EOS (Editor operating system). The current EOS prototype was used in the following two sub-projects within the project group UI.

The main goal of EOS is to provide an extendable, easy to use, and window system independent set of class libraries and tools, which enable the user to design and implement graphical editors. Unlike other User Interface Management Systems (UIMS), EOS assists the programmer of an editor not only by providing user interface elements, like buttons, menus or scrollbars, but mainly focusses on the drawing area part of an editor. Among the usual graphical functions, it also provides mechanism for active dialogue control with non-blocking input requests and supports a task- and semantics-oriented programming.

4.2.1.3 EXPREME

EXPREME is a joint development project between the project groups UI and SET. Figure 3 shows a screen dump of the current version of EXPREME. EXPREME is an easy-to-use graphical editor for the fast design of EXPRESS-G models. The user can annotate the graphic with all non-graphical EXPRESS features. This enables generation of

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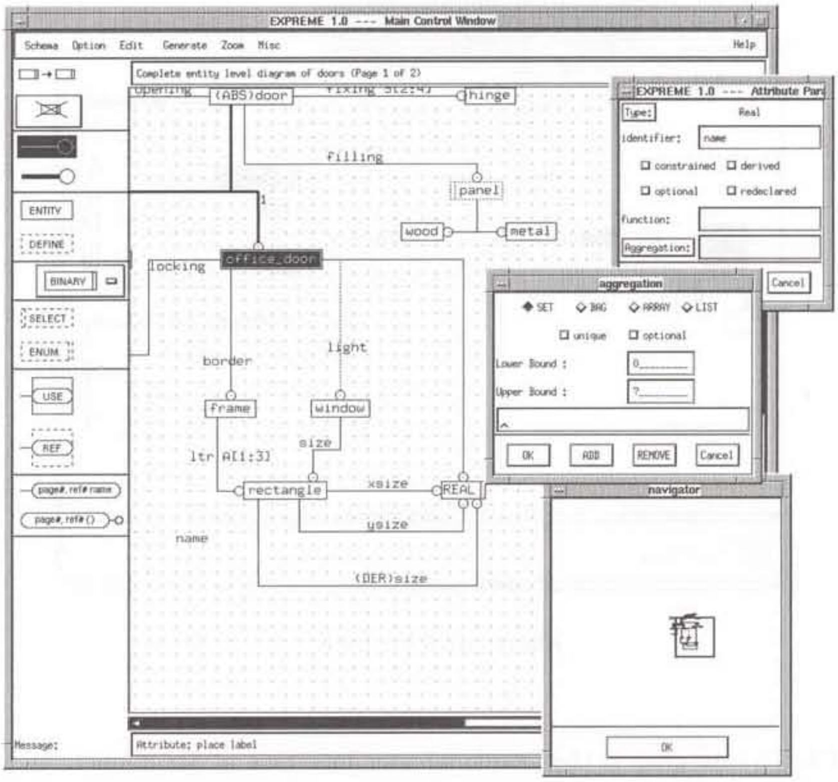

Figure 3: Screen Dump of EXPREME Editor

complete EXPRESS text. EXPREME recognises symbols on-line, prevents from drawing prohibited relationships or using reserved words as identifiers. Within the report period, the project group has strongly supported the development of the EXPREME editor. Many specific graphical utilities were implemented.

4.2.1.4 SCALOR

The second editor development activity, which has just begun at the end of the report period is the *SCALOR* Editor, which is required by the EMC-Workbench. The EMC-Workbench is used for the design and analysis of printed circuit boards for electromagnetic compatibility. Within the current EMC-Workbench, the LDA tool analyses a PCB layout for components and areas, where EMC problems may occur. Such components must be considered by corresponding EMC-arrangements. SCALOR is designed for supporting such arrangements within a PCB layout.

Within the report period, the implementation of the first release has begun. The development activities included the design of EOS-based classes for the graphical and internal representation of PCB layout components. The input format of SCALOR is SULTAN (Standard Universal Layout information Transport LANguage), which is developed in the Cadlab project group "Analog System Engineering".

4.2.1.5 Desktop

In the report period, the desktop development for SIFRAME 3.0 was an important

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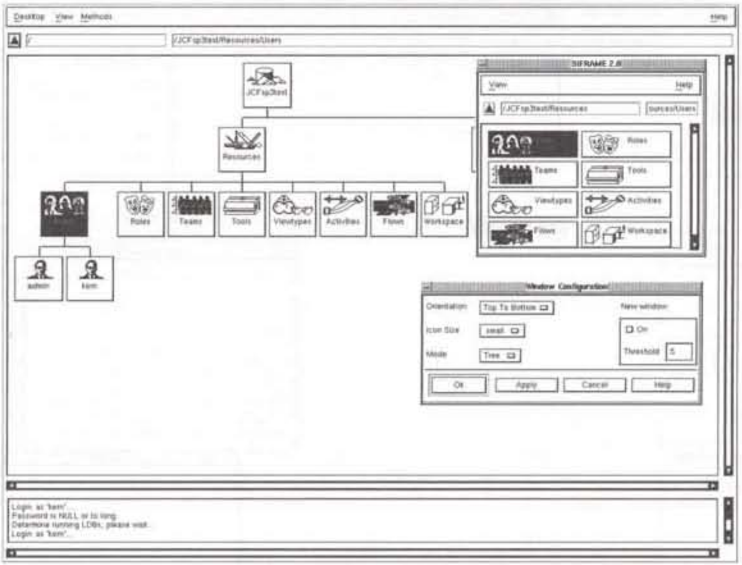

Figure 4: The *Desktop*

activity for UI. The desktop is the graphical user interface of SIFRAME. It provides top-level access to the designer's project environment, including project data and tools. Its user interface presents entities in an object-oriented way (see Figure 4). The *Desktop* uses the concept of

1. projects, which can be pieces of a design, libraries, tools or any number of other objects, and
2. the concept of methods, which can be simple commands, tools or other functions which are applied to the methods within the system.

The T30 milestone for SIFRAME 3.0 has been reached during the reporting period, the T50 is planned for the first quarter of '94. Since the participation of BT-UI in the development of the desktop will end after the T50 has been reached, some effort was spent to instruct and teach the people who will take over the development.

4.2.1.6 Other Activities

During the report period, a member of BT-UI also worked as a consultant for another SNI department. The goal of the project was to develop a Exhibition Information System based on X11, OSF/Motif and Informix.

4.2.2 Data-oriented Integration, DI

The work of project group DI is focussed on "Database Federation Services". This work is supplemented by research activities in the fields of tool integration environments and advanced database technology, e.g., object migration in federated database systems, views for object-oriented database systems, and transactions for design environments.

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In the following, more detailed descriptions about these single activities and their contribution to the DBF project, if applicable, are given. Main emphasis is put on the different phases and already available results within the DBF project.

4.2.2.1 The DBF Project

The "Database Federation Services (DBF)" project started in January 1993. The aim of the project is the federation of heterogeneous, autonomous database systems (DBS). Object-oriented database systems together with database systems based on the the most relevant relational or the entity-relationship model are candidates for the federation within the DBF project. DBF offers a solution in form of a flexible software layer on top of these heterogeneous database systems (see Figure 5).

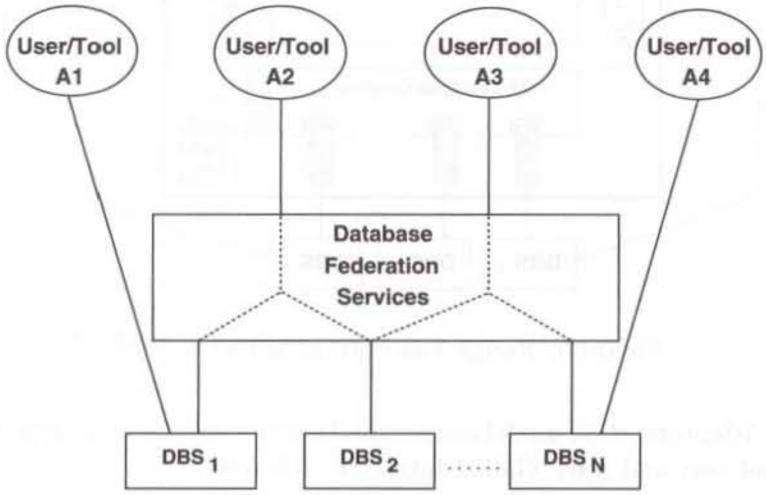

Figure 5: DBF System Model

It allows to preserve the autonomy of these "component databases (CDB)" so that their existing applications can continue to run locally (see A1 and A4 in Figure 5), i.e., no recoding is necessary (keyword: preservation of investment). On the other hand, it offers uniform and transparent access to the "federated data" of the CDB for new (global) applications (see A2 and A3 in Figure 5).

The DBF project follows the SNI Process Technology. The first phase of the project, called "Problem Analysis", was finished by delivering the DBF "Problem Space Specification (P30)" report, where a conceptual model for DBF (see Figure 6) and scenarios for productive use of DBF (see Figure 7 and Figure 8) are presented.

The DBF conceptual model contains the following modules:

- DB-Admin. Interface: supports administration facilities
- Global Interface: providing multiple federated and external schemata and furthermore operations according them; it is based on the ODL/OML (Object Definition Language / Object Manipulation Language) from the industrial standard ODMG (Object Database Management Group)

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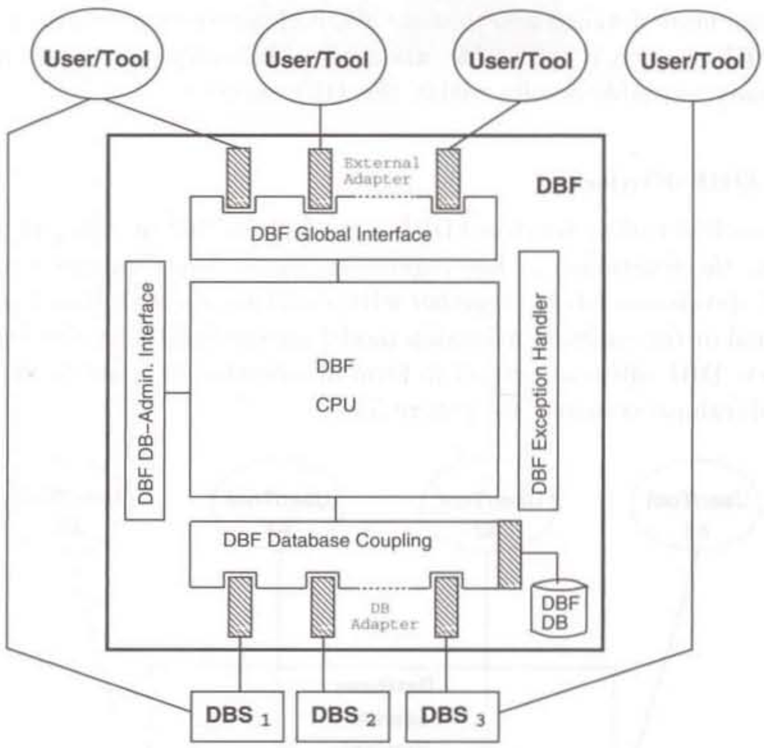

Figure 6: Rough Conceptual Model of DBF

- External Adapters: data model conversion between standard database interface used by a global user and DBF Global Interface – optional[7]
- Exception Handler: deals with anomalies like errors
- DBF CPU (kernel): connecting link between user resp. application and CDB, deals with necessary mappings and transformations
- Database Coupling & Adapters: data transport and conversion between heterogeneous, federated data base systems and DBF (with a canonical data model)
- CPU DB: storing global data, meta data and schema information of DBF

The application of DBF is not restricted to the federation of some database systems but DBF also supports two other solutions which have been identified to be required by customers:

- **Strong-Coupling:** full control over the CDB by DBF, no local users/applications, improved integrity for low level CDB, e.g., file system (see Figure 7)
- **Migration:** tool and data migration (see Figure 8)

In parallel to the "problem analysis" phase, the development of a DBF prototype has been started, in order to verify the basic concepts of DBF and to examine some other

[7] An External Adapter is only needed if the Global Interface and the user required database interface differ

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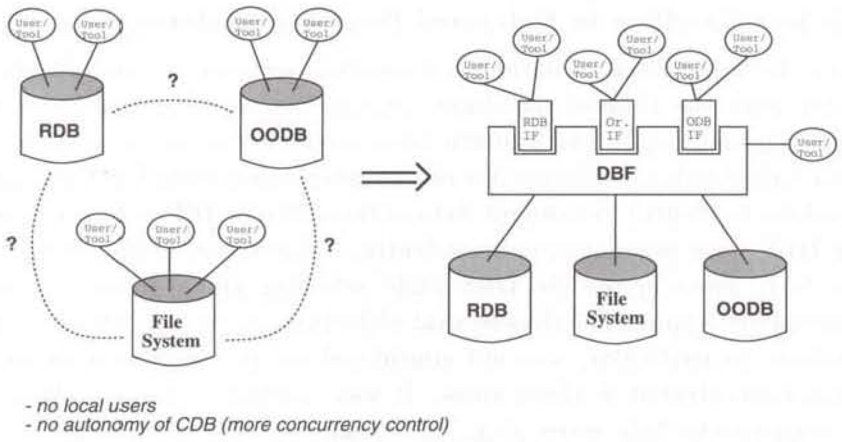

Figure 7: Strong-Coupling of CDB

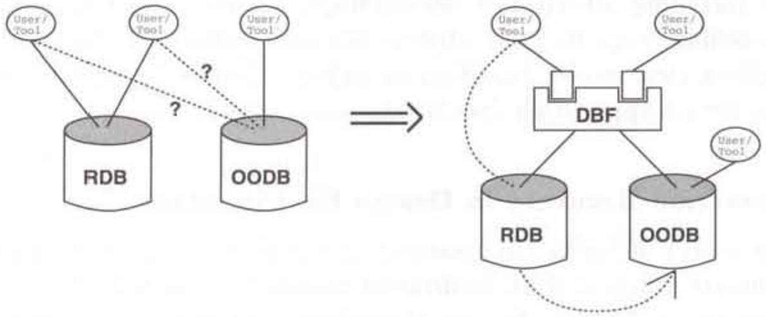

Figure 8: Tool and Data Migration

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issues. The prototype federates the object-oriented database SIFRAME-OMS with the relational database Entire. A first version was demonstrated to potential pilot users to illustrate first DBF features. Enhanced versions of the DBF prototype are planned for the future.

4.2.2.2 Object Handling in Federated Database Systems

To enhance the acceptance of database federation services, a comfortable handling of data (objects) from the coupled database systems has to be provided. A requirement study showed common topics like uniform transparent access on all data of the multiple DBS, but also raised enhanced issues like object integration and object migration. Object integration allows to identify redundant data of the different DBS which is often requested because the DBS were populated independently. Object migration, on the other hand, enables objects to move across the DBS while retaining global identity. An analysis of several existing DBF approaches showed that object integration is still under research and object migration, in particular, was not considered by any approach so far. Therefore, main research concentrated in these areas. It was completed by some base mechanisms for uniform transparent data access (e.g., for integrating their meta data).

This research activity is realized with many interactions to the DBF project. A primary problem analysis as well as base concepts are already adopted by the DBF project resp. will be used as input for future steps.

4.2.2.3 View Derivations in Object-Oriented Database Systems

Within the ANSI 3-level-architecture of database systems, views (also called: external schemas) serve to support a high degree of logical data independency and they may provide a more suitable and specific data representation to the different applications than it is offered by the global database description (also called: conceptual schema).

At Cadlab, current research activities concerning views are focussed on changing the data representation during the view derivation, i.e., during the step from the conceptual schema to the application specific views. Of special interest is the view specific handling of class lattices including inheritance relationships, complex objects, and a restructuring of the data modelling, e.g., to treat objects like attributes and vice versa. Aim of this work is to provide a view model, based on an object-oriented data model, to support a lot of opportunities for an application-specific data representation.

4.2.2.4 Transaction Recovery in Design Environments

An important aspect of design environments is the design transaction management. Design transactions are different from traditional transactions as they have to support long-lived and cooperative activities. Known algorithms for concurrency control and recovery are too restrictive for such environments. Thus, a lot of advanced transaction models have been developed throughout the last few years that try to support applications like design. A lot of those models focussing on the aspect of recovery, known to be an open problem for advanced transaction models, have been analysed. Traditional transaction management treats transactions as recovery units by simply aborting them in case of a failure. Such a simple mechanism is not adequate for long-lived and cooperative activities like design. Cadlab has therefore developed alternative recovery strategies, based on the transaction

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toolkit approach (developed at the University of Hagen) which allows the configuration of transactions in a very flexible way. Cadlab has also developed a prototype for the toolkit based on the JESSI Common Framework. The goal is to find primitives for recovery management that can be combined in an application-specific way to realize powerful recovery strategies.

4.2.2.5 Event-Trigger Mechanisms in Design Environments

Strongly related to design transaction management is the support of event-trigger mechanisms, which allow to define application-specific reactions (rules) to certain events. Such mechanisms are very general and can be applied for several typical problems, e.g., consistency checks, change notification or recovery. Because of their general nature, event-trigger mechanisms and their relationship to the transaction management are very complex. Typical problems are deadlocks, infinite loops or contradictions. Event-trigger mechanisms were analysed and basic elements were identified. It was necessary to restrict the use of those basic elements in an application-specific way in order to avoid an arbitrary and uncontrollable behaviour. This approach leads to the development of a typing mechanism for rules. Cadlab's goal is to further refine this approach and to integrate it with the transaction toolkit approach described above. This should result in a powerful concept allowing the application-specific definition of event-trigger mechanisms and their embedding in the design transaction management.

4.2.2.6 An Open Object-Oriented Integration Environment

Integration of tools into a design environment means to add tools into this environment and let them interact with other tools within the environment. This includes the organisation of data so that it can be shared by different tools as well as a common control mechanism for the coordination of control flow of tools. Whereas the organisation of data mostly is a structural aspect, the coordination of tools mainly is a behavioural aspect. Both aspects must be combined into a common abstract data model. The object-oriented approach supports both aspects in a proper way but it lacks a standardised object-oriented data model so far.

These were the requirements which led to the approach in this work. It presents an integration model containing object-oriented basic concepts which can be applied recursively to be configured to domain specific data models and data schemas. These concepts are as generic as to be still object-based and as specific as to allow the definition of particular concepts. As a result of the recursive approach the structural and behavioural coordination of different data models and data schemas as well as the definition of different application domains is handled in a unique manner. Based on these basic concepts different levels of tool integration as well as the integration of domain specific and domain neutral tools are supported.

4.2.3 Control-oriented Integration, CI

Within the report period the project IFS started with a problem analysis phase. This included several technical discussions with the partners both from community of knowledge based systems developers as well as end users of intelligent services. In this context the following result was produced:

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- "Statement of Problem" (P10) , May 1993

During work within the "Initial Situation Analysis" concrete ideas about user requirements, general constraints and possible solutions for the given problems were developed. One of the major results was that it is almost impossible to detect the real user needs for intelligent services unless the technical solutions are evaluated against a concrete application.

This led to the a redefinition of the project IFS by identifying two major sub-projects of IFS:

- IFS Basic Services
- IFS Application

4.2.3.1 IFS Basic Services

The work within IFS Basic Services contributes to the Applied Research part (SP1) and in the sequel to the Development part (SP2) of the JESSI Common Frame (JCF) project. Within this context cooperation started with FZI and Siemens ZFE within the subtask *Integrated Data and Knowledge Management* (IDKM). Work within this subtask lead to the definition of IFS Basic Services. These include a meta schema to represent hybrid knowledge, a hybrid knowledge description language (HyKL), an API to access and manipulate knowledge and a basic knowledge evaluation component.

Two JCF deliverables were finished during the report period:

- JCF/CADLAB/064-01/03-Nov-93 "Meta Schema for Hybrid Knowledge Representation and Management"
- JCF/CADLAB/065-01/02-Dec-93 "Theoretical Principles of Uncertainty Processing in Expert Systems"

The first document corresponds to a similar deliverable which was already produced by the partners in a former phase of JCF. The partner's document focusses on rule representation and management while the Cadlab document puts emphasis on hybrid knowledge representation to support the integration of the majority of knowledge based tools. A meta schema for hybrid knowledge representation is presented. This meta schema will support the integration of the frame concept with forward chaining rules and uncertainty handling. This meta schema shall be easily extendable to integrate further knowledge representation and processing paradigms (e.g. constraint handling).

Most knowledge based tools in the CAx area use either rules or frames to represent knowledge. Frames are the fundamental structure of choice for a wide variety of representational tasks. Each frame represents a concept, and consists of a collection of attributes, and their values, that are associated with that concept. In theoretical terms, a frame is simply the collection of assertions about a concept. In object terms, the frame is a mechanism for storing and retrieving the object-attribute-value triple for which the frame takes the first position.

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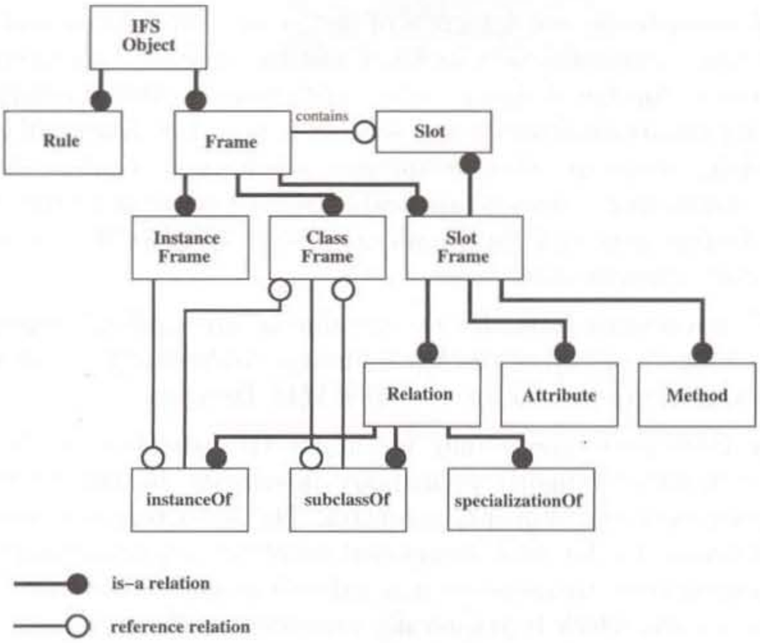

Figure 9: Meta Schema for Frame Representation

As shown in Figure 9, Frames are identified as either class frames, instance frames, or slot frames. These basic types are distinct.

The meta schema for frame representation is extended by rules and uncertainty handling.

The document "Theoretical Principles of Uncertainty Processing in Expert Systems" provides fundamentals about approaches to uncertainty processing. These include the probabilistic approach, an algebraic approach, the theory of evidence and an approach based on the fuzzy set theory which are described in the context of rule-based expert systems. Both the uncertainty processing itself, and its relationship to the factual knowledge and the rule base of an expert system, are presented along the same lines, to make apparent the similarities and differences between the approaches, as well as possibilities of their coexistence within the same system.

The theoretic foundations of the paper are used to develop a meta schema which provides representations deeply integrated with rule and frame representations. This will result in a specification of the HyKL language which is able to describe those representations and to operationalise them to be contained in a knowledge dictionary which is stored as a part of the SIFRAME database OMS.

4.2.3.2 IFS Application

Within the subproject "IFS Application" the hybrid knowledge representation schema has been evaluated by applying it to the problem of Intelligent System Design Support (ISDS) in the domain of Electromagnetic Compatibility (EMC).

The knowledge base of the ISDS application models parts of the electronic engineering domain relevant for the design of electronic subsystems and micro-systems with respect to EMC problems: The basic parts of this knowledge base are frame libraries for subsystems and wires, each structured by a hierarchical frame schema as shown in Figure 9. This

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schema controls consistency and integrity of instances. Subsystems and wires serve as components for new subsystems to be designed and are modelled by a number of technical attributes important for the design process. For example, norms constrain the design process with regard to standardisation and security issues. A designer will interact directly with this knowledge structure when he specifies a new case: That is, describing a new subsystem by constructing it from components already persistent in the knowledge base. Another kind of interaction with the knowledge base is to instantiate the frame structure with further norms, wires or subsystems.

In this sample application forms for the creation of wire and subsystem instances are implemented as widgets on top of the Motif library. Additionally a user can browse the subsystem and wire hierarchies within the SIFRAME Desktop.

Although the ISDS prototype is only meant for the validation of the frame part of HyKL, the user interface supports preliminary inferencing by the representation of so called influence matrices and frequency schemata. The latter represent radiation emission and irradiation sensitivity for each component involved in a configuration. From this, the mutual disturbance of components in a subsystem can be estimated and registered in the influence matrix, which is graphically presented to the user beside the frequency schemata. Most of the graphical interface objects are context-sensitive with regard to mouse and keyboard actions. Future versions will also take advantage of the possibility of using rules and uncertainty with HyKL.

4.3 Summary and Outlook

In Base Technology a new research and development programme has been successfully initialised with the goal of further extending the capabilities of the JESSI Common Framework JCF/SIFRAME with new basic CACE services. Besides providing functional extensions to JCF/SIFRAME, the new CACE components can also be used outside JCF/SIFRAME, i.e., in case of the DBF project, to offer support for the integration and coupling of external frameworks and CAx-Systems as well.

In the report period, the problem space of CACE/BT was investigated and projects on "Data Base Federation, DBF", "Advanced Editing Systems, AES", and "Intelligent Framework Services, IFS" were started. Apart from delivering basic software documents as specified in the SNI process technology, in all projects prototypes were built and discussed with potential industrial users. These prototypes included to a large extent the results of research work performed in previous report periods.

In AES, a prototype editor operating system EOS was built and applied to the construction of the EXPRESS-G systems editor "EXPREME". Within the DBF project a first prototype for coupling relational and object-oriented data bases was built. Starting from the task of coupling heterogeneous, distributed databases, DBF will also offer services and strategies for stepwise transforming heterogeneous systems into uniform ones by means of migration (this has been found to be a very strong user requirement). In IFS hybrid knowledge representation services have been conceived. Prototyping here focussed on EMC consultancy.

In parallel to these development oriented activities, further applied research work was carried out in the mentioned areas as well as in "design transaction management" and "object oriented integration". Here, a series of PhD theses are to be expected.

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In the next report period first software releases are planned in the projects DBF, AES and IFS. The corresponding components will then be integrated into JCF/SIFRAME. Strong cross-fertilisation is expected from further intensive customer contacts, participation in various European R&D projects, as well as from internal collaboration with System Engineering Technology, SET, and Analog System Engineering, ASE.

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5 System Engineering Technology

5.1 Introduction

The System Engineering Technology Group (SET) performs research and development in the field of concurrent system engineering. The target is the development of integrated generic environments for system development and system control. Accordingly, the term "concurrent system engineering" denotes both "the engineering of concurrent systems" and "the concurrent engineering of systems".

5.2 Baseline

Since information technology plays a key role in linking several technologies like mechanics, communication, transport, business etc., system engineering environments have to consider these application domains and should not be restricted to hardware or software systems. Cadlab came to the conclusion that as a basis for system engineering environments with these different application domains, in a first step an integrated core environment needs to be developed. The model, methods and tools of this core environment must be largely independent of the envisaged application domains. In a second step the core model and the methods have to be specialised and system engineering environments including process control mechanisms for different application domains are to be realized. Nevertheless, it is not reasonable to develop the core model and methods independently from existing problems in any application domain. Therefore, in the first step systems and engineering strategies in mechatronics, telecommunications and hardware engineering must be considered.

A crucial point for the acceptance of the domain specific environments by the system engineer is its graphical user interface. The user interface should provide the system engineer with the system representations she or he is familiar with. In mechanics, for instance, EXPRESS plays an important role for the specification of product data models, in the telecommunication domain SDL is widely used for system specification. For hardware engineering VHDL is the standard specification language.

Another important factor to be considered for system engineering environments is the increasing complexity of systems. In order to cope with this factor, the use of concurrent design methods that shorten the design cycle is required. Just a collection of tools cannot support concurrent design effectively, even if these tools are integrated. Therefore methods for the control and guidance of the engineering process are needed.

5.3 Work During the Report Period

During the report period the group SET worked in the fields of:

- system specification and evaluation
  - mechatronics systems
  - research on the formalisation of distributed backplane-based simulation with extended Petri nets
  - design assistance

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- development of an EXPRESS/STEP Environment
- hardware design methodologies
  - hardware synthesis
  - VHDL activities
  - handling of asynchronous hardware
  - timing analysis
- evaluation of the JESSI-Common-Framework
- simulator generation (GRAPES Simgen)

5.3.1 System Specification and Evaluation

Current information technology is frequently used within complex real world systems consisting of a lot of different components with quite different characteristics. For example, mechatronics systems can be divided into the physical system and the information technology part (cf. Figure 10). The information technology part itself can be further divided into the digital system for general calculations and the control system, which is responsible for the control of the physical part. In order to develop such heterogeneous systems it is no longer possible to handle and develop each system component on its own, but all the other system components have to be considered when developing one specific component. The sequential development of the different components where the designer uses the already existing development results of the other system components for the work is very time consuming and leads to bad results concerning time to market. Thus, it is necessary to develop the different system components concurrently. But, while performing this concurrent development, also the other system components have to be considered as much as possible. Usually, however, the various system components are described quite differently.

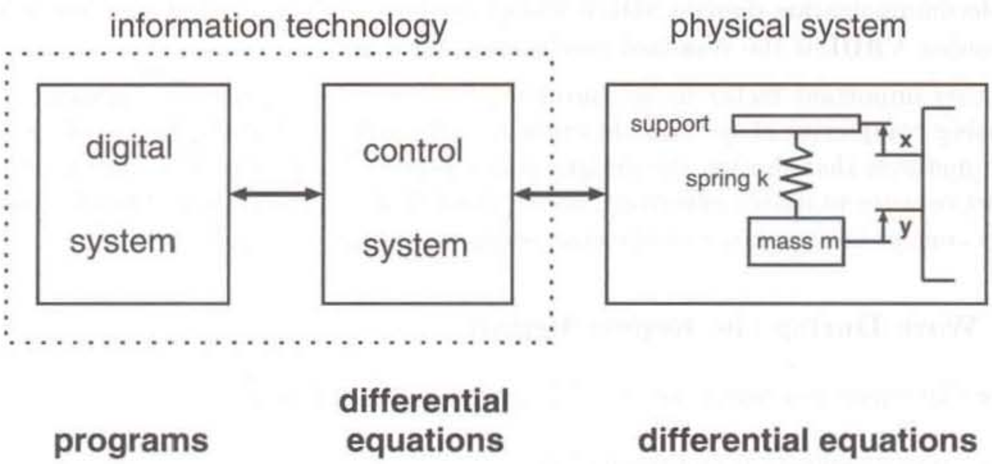

Figure 10: Different Parts of a Heterogeneous System

The use of this variety of specification techniques leads to problems during simulation and analysis of a component when regarding the interface to the surrounding system.

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Thus, the requirement for a homogeneous model and a uniform specification technique for heterogeneous systems arises.

On the other hand, it can not be expected that such a new uniform specification technique will be generally accepted among the designers of the different areas. These contradictory requirements can only be met by providing the designers of the different system components with the specification technique they are familiar with but transforming all these different specification techniques into a uniform internal model. Of course, this internal model can also be directly used for the specification of some of the system components. Therefore, the software architecture of Figure 11 has been developed.

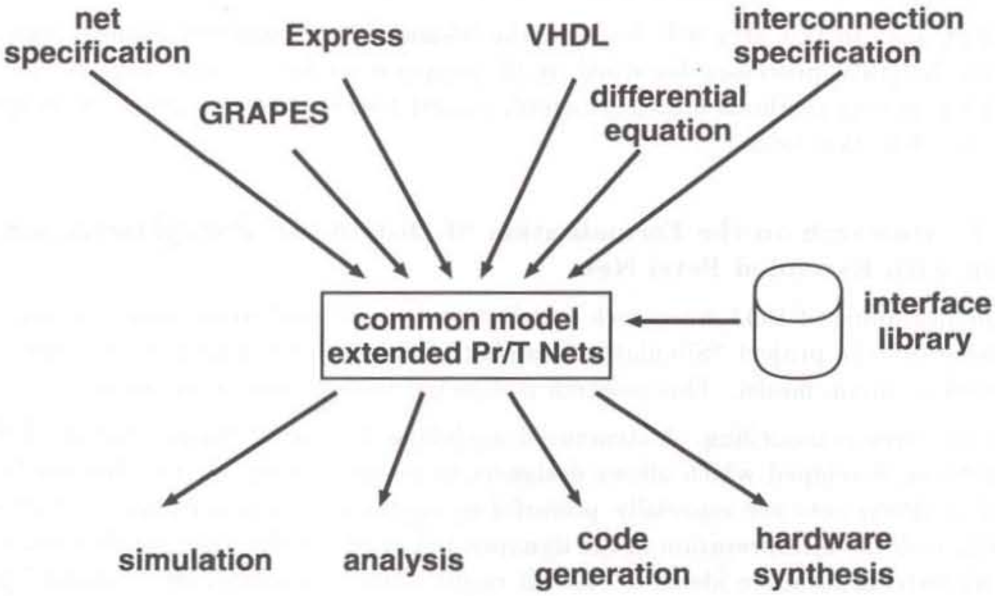

Figure 11: Software Architecture for the Concurrent Design of Heterogeneous Systems

The center of this architecture is the common model which is based on extensions of timed Predicate/Transition nets. But as input the different modelling paradigms the designers are used to are accepted. For the specification of the software part of the heterogeneous system this might be GRAPES whereas the control system might be described by differential equations. For the transformation of the different specifications into the common model already existing tools, for example for the discretisation of the differential equations, can be used. The interconnection of the system parts can be directly specified with the common modelling technique or can be extracted from a library developed for this purpose. Thus, all parts of the system are described in the common model, which is used as a base for different tools, for example for simulators, analysers, code generators and so on. For these tools it is no longer relevant which modelling paradigm has been used by the designer for the specification of a special part of the system.

5.3.1.1 Mechatronics Systems

Within the report period mechatronics systems were especially regarded. These systems typically consist of digital components, physical components and control components connecting these two kinds of components. Both, physical components and control components show analogue behaviour which can be described by differential equations.

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The digital components are usually described by algorithms. Based on the timed Predicate/Transition nets of the common model a methodology was developed which allows the specification of the analogue components of a mechatronics system, too.

Because of their high performance and scalability massive parallel systems become more and more important for the realisation of mechatronics systems. Especially, real time conditions have to be considered. To guarantee hard real time deadlines, the operating system overhead has to be minimised. For this purpose it is very useful to pre-analyse the application in order to configure the operating system. Usually, complex real-time applications involve many processes which behave very static (i.e., their run time and their communication requirements are deterministic).

Further work in this area will focus on the design of a suitable pre-analysis tool which analyses the static processes described by the common model. For this purpose the hardware development methods *high level synthesis* and *timing verification* will be adapted to the new application field.

5.3.1.2 Research on the Formalisation of Distributed Backplane-Based Simulation with Extended Petri Nets

In the beginning of 1993, a research activity has been started to combine the results and experiences of the project "Simulator Coupling" finished in 1992 with the emerging Petri net-based common model. This research is directed towards two main areas.

The first area is modelling. A structured modelling framework based on extended Petri nets is being developed which allows designers to model systems on well-defined levels of precision. Petri nets are especially powerful in capturing non-determinism. However, a problem with the interpretation of the dynamic behaviour of Petri net models arises when some underlying intuitive ideas, of "how it could work" are sort of an "invisible" part of the model, which can lead to serious misinterpretations. The modelling concept pursued is to provide a modellers' library of Petri net models to incorporate certain aspects of the dynamic behaviour, especially to enable a precise notion of non-determinism in some way. An example is the issue of fairness.

The second main aspect of this research is the application of the modelling framework to the formalisation of the CFI standard for simulation backplanes. When it comes to standard interpretation and validation of standard compliance, the above mentioned ambiguities of the dynamic semantics of the model become crucial. The research goal is to derive from the modelling framework a validation concept to check whether either a simulator or a simulation backplane implementation meets the standard.

Currently, the basic structure of the modelling framework has been designed. The modelling of the CFI simulation backplane standard will start in February 1994. Major results are expected by the end of 1994.

5.3.1.3 Design Assistance

During the report period, DECOR, a configurable design flow management component that supplements a framework by services for online monitoring and control of concurrent design processes, was revised. With online monitoring each member of a concurrent working team knows the actual state of every object he wants to manipulate. This avoids

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unnecessary locking of objects that causes sequentialising of design tasks that could otherwise be performed in parallel. In addition, services for automatic execution of design actions are provided. The design management component is tightly integrated into the JESSI-Common-Framework like a usual design tool. Furthermore it is based on extended Predicate Transition Nets as modelling paradigm, which allow a clearly defined specification of concurrent behaviour. DECOR consists of a Net Editor for the specification of concurrent design processes with extended Predicate Transition Nets and an Execution Monitor with User Interfaces. The Execution Monitor handles the online monitoring and control of the design processes.

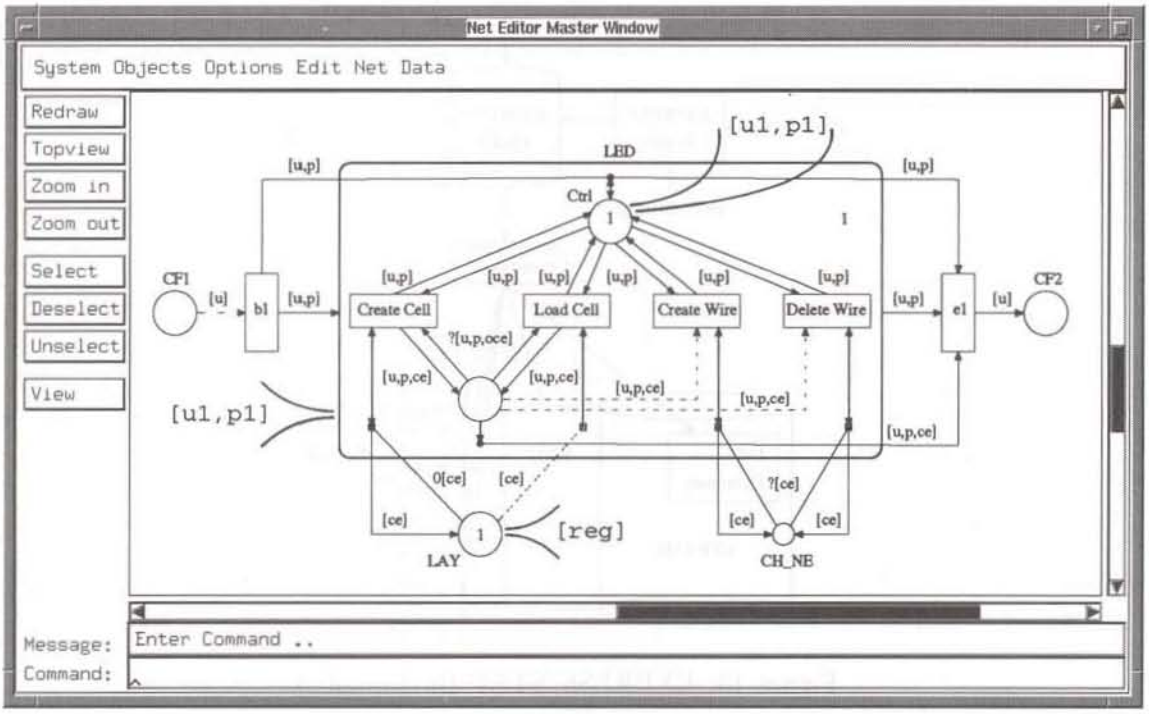

Figure 12: Screen Dump of the Net Editor

5.3.2 EXPRESS/STEP Environment

Based on the work performed in ECIP2 (European CAD Integration Project) WP1, the group SET started the project EXPRESS/STEP Environment in the beginning of 1993. The ECIP2 project was successfully finished by the end of June 1993. The main key deliverable within WP1 was the prototype of a complete EXPRESS Modelling Environment including an extended EXPRESS-G editor, an EXPRESS-G layouter, an EXPRESS reader, and an EXPRESS text generator. The remainder of this paragraph only refers to the recent activities of the new EXPRESS/STEP Environment.

The ISO 10303 standard ("Product Data Representation and Exchange") is usually called STEP. The main parts of STEP are:

- Description Methods
- Implementation Methods

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- Resources
- Application Protocols

The basic idea of this project is the generator approach. Since an EXPRESS model automatically defines a file format for data exchange and a database interface, the corresponding STEP software can be generated automatically from EXPRESS models (cf. Figure 13 for an overview).

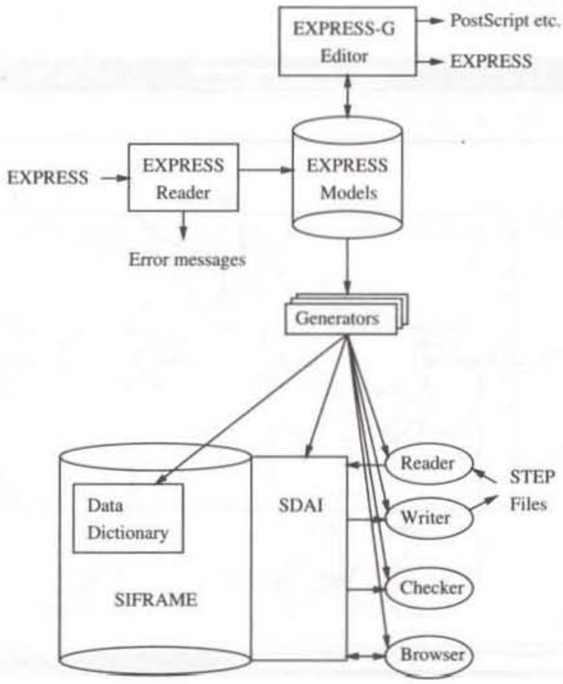

Figure 13: EXPRESS/STEP Environment

The input for the generators are EXPRESS models. Three tools are needed for handling the EXPRESS models:

EXPRESS-G Editor for creating and modifying EXPRESS models.

During the report period, the EXPRESS-G editor EXPREME (see Figure 14) was developed, employing EOS (see Section 4.2.1.2). EXPREME is an easy-to-use EXPRESS-G editor for the fast design of EXPRESS models. The graphics can be annotated with all non-graphical EXPRESS constructions, enabling the generation of complete EXPRESS models. EXPREME checks inputs on-line, thus prevents users from using illegal identifiers or drawing prohibited relationships, etc.

EXPRESS Reader for reading and checking EXPRESS models.

During the report period, the EXPRESS syntax and semantics checker ICE was developed. Since November '93, ICE is available free of charge for Sun-4, SGI, HP9000, Apollo, IBM RS6000, OS/2, and Linux. The ICE software can be retrieved from the ftp server of Paderborn University via anonymous ftp.

Model Manager for managing the EXPRESS models.

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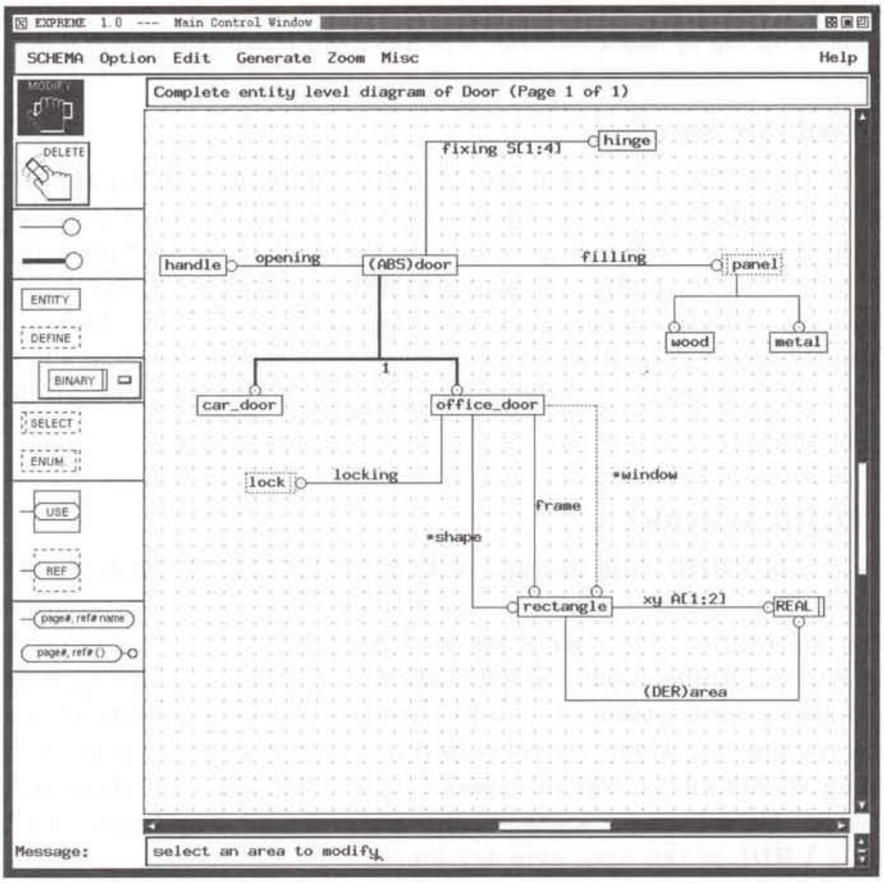

Figure 14: EXPREME

These tools are not only the basis for the EXPRESS/STEP Environment, but can also serve as an independent EXPRESS modelling environment.

The EXPRESS models are the input for all kinds of generators:

- a generator that initialises a data repository with a dictionary containing the required EXPRESS models and creates an SDAI procedural interface to this repository,
- a generator that creates a reader and a writer for STEP files that correspond to an EXPRESS model,
- a generator that creates a data browser.

During the report period, the work on the SDAI generator was started.

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5.3.3 Hardware Design Methodologies

The work in this field can be further split up into the areas *hardware synthesis*, *VHDL activities*, the *handling of asynchronous hardware*, and *timing analysis*.

5.3.3.1 Hardware Synthesis

The work on the hardware synthesis project OMSI (Optimised Model Transformations at the Synthesis of Digital Information-Processing Systems) was continued during the report period. In this project, Cadlab cooperates with Ilmenau Technical University, Humboldt University Berlin, and the GMD. The goal of OMSI is to improve the interactions between synthesis phases. Together with Ilmenau Technical University, the logic synthesis tool CLASSY and the layout generator GeLaS were combined in order to build a fully automatic generator of datapath layouts. Furthermore, new algorithms for topological compaction were developed.

5.3.3.2 VHDL Activities

The work in the VHDL work package of ECIP2 (European CAD Integration Project) was finished in September. In this project, Cadlab cooperated with different industrial partners and universities. The goal of the work package was to promote the VHDL standardisation within Europe. Common application subsets and packages, design guidelines and methodologies were examined. Cadlab worked on the feasibility of a multi-kernel simulation environment, where several (arbitrary) simulation kernels are coupled within a surrounding simulation system to support the cooperative simulation of a single and uniform design. Guidelines for a general multi-kernel modelling language and a sample application of VHDL in this area were developed.

The work in the standardisation area of VHDL has been continued in the ECIP2 successor project ESIP (EDA Standards Integration and Promotion) which started in October. In cooperation with the Swedish partner Synthesia, Cadlab will concentrate on building a bridge between VHDL and emerging specification methods.

Further contribution have been made to the balloting of VHDL92 as well as to the Balloting of the Std_Logic_1164 (IEEE PAR 1164). Finally, research has been started in order to define the High-Level semantics of behavioural VHDL.

5.3.3.3 Handling of Asynchronous Hardware

During the report period, a methodology for the synthesis from a VHDL algorithmic description to an interconnection of asynchronous automaton was developed. For this purpose, the translation of VHDL algorithms into simple Petri nets as well as Predicate/Transition nets was developed. For the hardware realization, an asynchronous automaton architecture was developed to cover the Petri nets derived from the specification.

A special feature of the automaton architecture is the realization of any arbiter specification.

The relation between the specification and the synthesis result is formally defined by using trace structures, which model the interface behaviour of the hardware to be synthesised.

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5.3.3.4 Timing Analysis

The Cadlab Timing Analysis System (CaTAS) is an advanced timing verification system which provides a unique, powerful approach to help the user to detect timing problems such as set-up, hold, and minimum-pulse-width timing violations. It uses stimuli-independent timing analysis techniques to get fast, accurate timing reports. CaTAS consists of two different main parts: a batch system TIV and an interactive system FATIMA.

During the report period work focussed on CaTAS' interactions with Cadlab's EMC-Workbench, i.e., to get timing information from the LDE/LDA to include EMC-caused timing effects into the timing verification step. Furthermore TIV was improved with respect to run time and memory limitations, and FATIMA was enhanced with further functionality.

Furthermore, some work in the combination to timing analysis and the common model was performed. The common model allows to check timing constraints and requirements on higher levels of abstraction. This results in the ability to use a level and application independent Petri-net simulator, and leads to the new concept of static *level-independent timing verification*, which is the application of static methods to detect timing problems independent from the level of abstraction.

5.3.4 Evaluation of the JESSI-Common-Framework

Within the project 'JESSI COMMON FRAME' the task of sub project 4 (SP4) is to evaluate current releases of the framework software and to derive requirements for future releases. In 1993 several framework releases were handed on to SP4, JCF R2.0, JCF R2.1, and JCF R3.0 in a preliminary version. All these releases were delivered as complete systems without providing lower level interfaces, i.e., tight integration is not yet supported by the framework. Within SP4 the evaluation is therefore still based on the encapsulation of tools into the framework. Cadlab contributed to this work in many ways.

- All delivered releases were installed and first hands-on experiences were gained through the encapsulation of simple Unix tools.
- The synthesis system PASS was encapsulated in JCF and in this form delivered to the Joint Evaluation Design System (JEDS).
- The performance of JCF R2.0 and JCF R3.0 was quantitatively measured.
- A detailed evaluation report on JCF R2.0 was written.
- Several requirements for JCF R3.0, JCF R3.1 and JCF R4.0 were stated, considering especially aspects of tight integration.

5.3.5 Simulator Generation (GRAPES–Simgen)

Cadlab's GRAPES-Simgen-II[8] (GRAPES-Sim-Generator-II) project is the second part of a cooperation with SNI AP 231. In order to simulate GRAPES models using the MODSIM-Simulator, GRAPES-Simgen is one link in the transition from GRAPES-diagrams to the

[8] GRAPES is a registered trademark of SNI.

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simulator. Simgen cross-compiles GRAPES-PRSIM to GRAPES-SIM, and collects information on how the compilation is done. The project was initially planed for the first half of the report period. Due to further requirements it's end was postponed until December 1993.

5.4 Summary and Outlook

Most of SET's activities concern the concurrent design of heterogeneous systems. Figure 11 shows the software architecture that was developed for this purpose. The center of this architecture is the common model which is based on extensions of timed Predicate/Transition nets. But as input the different modelling paradigms the designers are used to are accepted. During the report period, mechatronics systems were especially regarded. These systems typically consist of digital components, physical components and control components connecting these two kinds of components. A methodology was developed which allows the specification also of the analogue components of a mechatronics system. The Predicate/Transition-nets model has been used also for modelling design processes in order to enable design assistance.

A further activity has been the development of the EXPRESS/STEP Environment. During the report period, the EXPRESS-G editor EXPREME (see Figure 14) was developed. EXPREME is an easy-to-use EXPRESS-G editor for the fast design of EXPRESS models. The graphics can be annotated with all non-graphical EXPRESS constructions, enabling the generation of complete EXPRESS models. EXPREME checks inputs online, thus prevents from using illegal identifiers or drawing prohibited relationships etc. Furthermore, the work on the SDAI generator for SIFRAME was started.

In the field of hardware design methodologies, work was continued on the hardware synthesis project OMSI, the VHDL work package of the ESPRIT projects ECIP2 and ESIP, timing analysis, and the synthesis of asynchronous hardware.

Within the project 'JESSI COMMON FRAME', sub project 4, several framework releases (JCF R2.0, JCF R2.1, and JCF R3.0) were evaluated, and requirements for future releases were derived.

Cadlab's GRAPES-Simgen-II project is the second part of a cooperation with SNI AP 231. The project was initially planed for the first half of 1993. Due to further requirements it's end was postponed until December 1993.

In 1994, the following will be undertaken:

- Design and development of a data schema for the common extended Predicate/Transition-net model. The model will cover hierarchy, the handling of sets, and timing.
- Development of the EXPRESS/STEP Environment will be continued. In 1994, the first tools will be completed.
- The hardware synthesis project OMSI will be completed in 1994. The work within the VHDL work package of ESIP, timing analysis, and the synthesis of asynchronous hardware will be continued.
- Within JCF SP4, the evaluation of new JCF releases will continue, in particular with respect to tight integration of tools.

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6 Analog System Engineering

The objective of the "Analog System Engineering" group is the development of software tools and methods for the design of electronic circuits and systems with respect to their Electro Magnetic Compatibility (EMC).

The main task is the development and production of the EMC–Workbench for the design and analysis of printed circuit boards under EMC constraints. This workbench consists of different tools for placement analysis, layout data extraction and pre-analysis, calculation of transmission line parameters, simulation of reflection and crosstalk effects, simulation of radiation and irradiation, and for a graphical post-processing of simulation results and measurement data. Also an EMC–library which contains macro-models for digital components is part of the EMC–Workbench. Another scope of work is the development of a generalised design process for arbitrary systems and micro–systems taking also into account their Electro Magnetic Compatibility. This includes the consideration of EMC during the planning of systems. It is intended to use the gained knowledge for the design and development of an Microsystem–Workbench. Furthermore, there are a lot of activities in the development of macro-models for analog components which are necessary for a fast and accurate simulation of analog circuits and analog printed circuit boards. In the following, the baseline of the work carried out during the report period is summarised.

6.1 Baseline

6.1.1 EMC–Workbench

The EMC–Workbench is an analysis environment for the design and analysis of printed circuit boards considering the Electro Magnetic Compatibility. With the development kit of SIFRAME different tools for simulating and analysing EMC–effects like reflection, crosstalk, radiation, irradiation, etc. are integrated to get an homogeneous and comfortable environment. Using this software, design errors caused by EMC–effects, can be detected before prototyping during the design and therefore, the number of re-designs will be decreased as well as the product quality will be improved. The results are shorter time to market and lower development costs. The application of the EMC–Workbench within the complete design process of systems and modules is an example for concurrent engineering.

In addition to the continuous improvement of the simulation algorithms and user interfaces of all tools of the EMC–Workbench some important new tools and algorithms were developed and implemented.

- The simulation of the electrical behaviour of circuits and systems requires the knowledge of the dynamical behaviour of all components involved. To provide this information in an efficient way to the different simulation and analysis tools of the EMC–Workbench (e.g., FREACS, LDE/LDA, MANDI, COMORAN, future rule based advisory system) a first version of an EMC Component Library has been defined, specified, and implemented. The structure and the necessary standardised interfaces have to be designed in such a manner that connections to different external databases and to different tools of the EMC–Workbench are possible.

- To provide within the EMC–Workbench a time efficient reflection analysis of printed circuit boards, the complete analysis process can be divided by the user into a fast

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and approximate pre-analysis and an accurate simulation of those electrical nets which have been detected as critical during the pre-analysis. The reflection pre-analysis can be carried out very fast by a worst case estimation of the maximum overshoot and undershoot which will occur at the receivers of the examinated nets.

The EMC–Workbench is used by several electronic design departments of SNI in order to improve their designs and products with regard to EMC. Layout data of digital printed circuit boards were analysed in order to detect disturbing reflection and crosstalk effects. Furthermore, the size and the arrangement of apertures within computer boxes were optimised to minimise the radiation of the complete system. These cooperations with the development departments have many advantages. On the one hand the time to market and the development costs of the products are decreased and the product quality is improved. On the other hand the application of the tools within real life development processes gives important feedback to improve all tools with respect to their applicability and their handling (e. g., user interface, necessity of additional features).

6.1.2 Microsystem–Workbench

In general a micro–system consists of different components of different scopes like micro-mechanics, micro-electronics, micro-fluiddynamics, micro-optics, and micro-acoustics. The design of components of different scopes requires the support of different design and analysis tools, which may be based on completely different methods. Furthermore, some tools are necessary which work on systems level. These facts lead to a very complex structure and an inhomogeneous set of tools.

Therefore, the designer of systems and micro-systems requires the support of software which is able to manage this inhomogeneous set of tools and the amount of design and analysis data which will occur during the complete design and developing process. This support can be provided in an efficient manner employing a framework with an object oriented database. To support the design of all kinds of micro-systems and systems a first step is the definition and development of a generalised design process which will be the basis for the requested design environment called Microsystem–Workbench.

6.1.3 Analog Macromodelling

Electronic systems contain more and more analog and mixed digital/analog circuits and printed circuit boards. The accurate simulations of the electrical behaviour as well as the noise behaviour of these circuits can be carried out by the consideration of the detailed internal structure of the analog components which can be given by a SPICE description on transistor level. As this procedure leads to very time consuming calculations the dynamical behaviour of analog components can also be described by models with an easier structure which are called macro-models.

An efficient modelling technique for analog components is based on the block–oriented modelling approach. Using this method the model is composed into different stages which can be reused within other applications. The different stages can be modelled independent from the internal structure of the component. The modelling is solely based on functional aspects and of course on the technology.

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6.2 Work During the Report Period

In the current report period the overall work on Electro Magnetic Compatibility was supported by the two national funded JESSI projects AC–5 "Development of an EMC–Workbench for Microelectronic Application" and AC–12 "Analog Expert Design System".

Within the project AC–5, which is coordinated by Analog System Engineering, new tools for the design of printed circuit boards and systems under EMC–constraints were developed. Furthermore, methods to consider EMC–effects during the planning phase of systems were investigated. The achieved results and experiences will be needed in the future to develop corresponding advisory tools. Effort has been spent among others for the specification and implementation of a first EMC component library, the development of new macro-model structures of digital components, the improvement and further development of the radiation tool COMORAN including investigations on the development of application rules, and the improvement and further development of the tools FREACS and TALC. Excellent results, reporting to JESSI and the national funding authorities as well as the annual review of the project work by the JESSI Sub-Management Board – Application (JSMB–A) lead to a relabelling as a category I project (project with no problems) of AC–5.

The work within AC–12 is focussed on modelling and the EMC–analysis of analog circuits. The work was concentrated on the development of simulation strategies for the acquisition of knowledge about noise behaviour of analog devices and methods for modelling of parasitic effects. A strategy was elaborated to include parasitic effects into the simulation of typical applications and on how to analyse the reaction of these effects on integrated circuits. Furthermore, effort was spent in the development of macro-models for analog components on behavioural level taking into account parasitic effects. A first set of building blocks, consisting of a multiplier, a comparator, and a timer, was modelled. Just as AC–5, also AC–12 was relabelled as a category I project.

System Engineering is involved in three national projects, "Examinations in Micro–system Design (MST–UEM)", "Methods and Tools for Micro–system Design (METEOR)", and "Model–library for Complex Analog Components (MST–BIB)". These projects are part of micro–system activities of the German Ministry for Research and Development (BMFT).

Furthermore, within the report period two new projects have been launched. The project "Online Placement on Printed Circuit Boards" is dealing with the development of fast parallel algorithms for the detection of noise effects on printed circuit boards. Within the project "Quality Assured PCB–Design under EMC–Constraints" strategies for an optimisation process for the placement of capacitors on printed circuit boards will be developed.

6.2.1 EMC–Workbench

6.2.1.1 EMC Component Library

The simulation of EMC effects requires an EMC component library for use in the EMC-Workbench. This library has to contain all EMC relevant data like:

- administrative data (identification number, case type, etc.),

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- pinning data (information about the function of the pins to generate an appropriate macro-model), and
- electrical (e.g. Vcc) and measured data.

The EMC component library will be used by various tools like FREACS, LDE/SIG, MANDI, COMORAN, and by the rule based advisory system, which will be a future extension of the EMC–Workbench.

During the report period the work was focussed on the definition of the library structure. A preliminary structure including standardised interfaces has been worked out. The provisional library structure and the necessary connections to the EMC–Workbench are shown in figure 15.

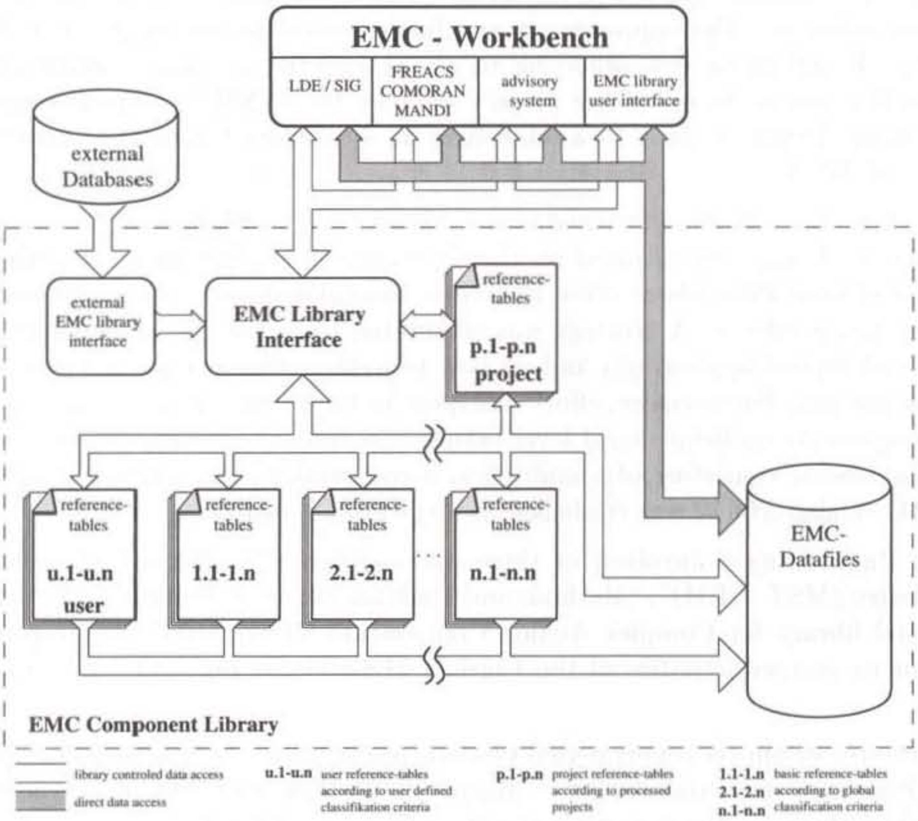

Figure 15: Preliminary Structure of the EMC Component Library

The tools of the EMC–Workbench, which use specific component data, access data using the EMC library interface. Every access to get information out of the EMC component library will be controlled by this interface.

The user will be enabled to complete and manipulate the library data by using an EMC library interface. The EMC library interface will also communicate with the EMC component library by using the EMC library interface. In this way, using the EMC library interface, the user will be guided to do any relevant library action (data check in, data check out, etc.).

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An external EMC library interface allows data transfer from external databases to the EMC component library. To ensure that a lot of different databases can be connected, the external EMC library interface is freely configurable.

Data queries to the EMC component library are served by using "reference tables". A reference table describes the structure of a component and contains pointers to associated simulation models. These simulation models can be accessed by tools directly.

Furthermore, the concept of reference tables contains so-called project reference tables, which will be created automatically for each project. A project reference table will include all project specific references. By this method the user is enabled to manipulate project specific data references, e.g., to experiment with certain aspects like configurations or technologies, without changing the basic reference tables. A newly created reference table can be transferred into a basic reference table by the EMC library user interface.

The format of reference tables is based on a consistent schema to define information types by names, called HINAC (**HI**erarchical **NA**ming **C**onvention). These names, containing the information as pointers to data files, are realized as strings (HINAC string). For user manipulations a separate user reference table is maintained to guarantee the consistency of the EMC data. This schema allows a flexible and compact representation of structured information. The use of the hierarchical naming convention (HINAC) provides the necessary expansion capability.

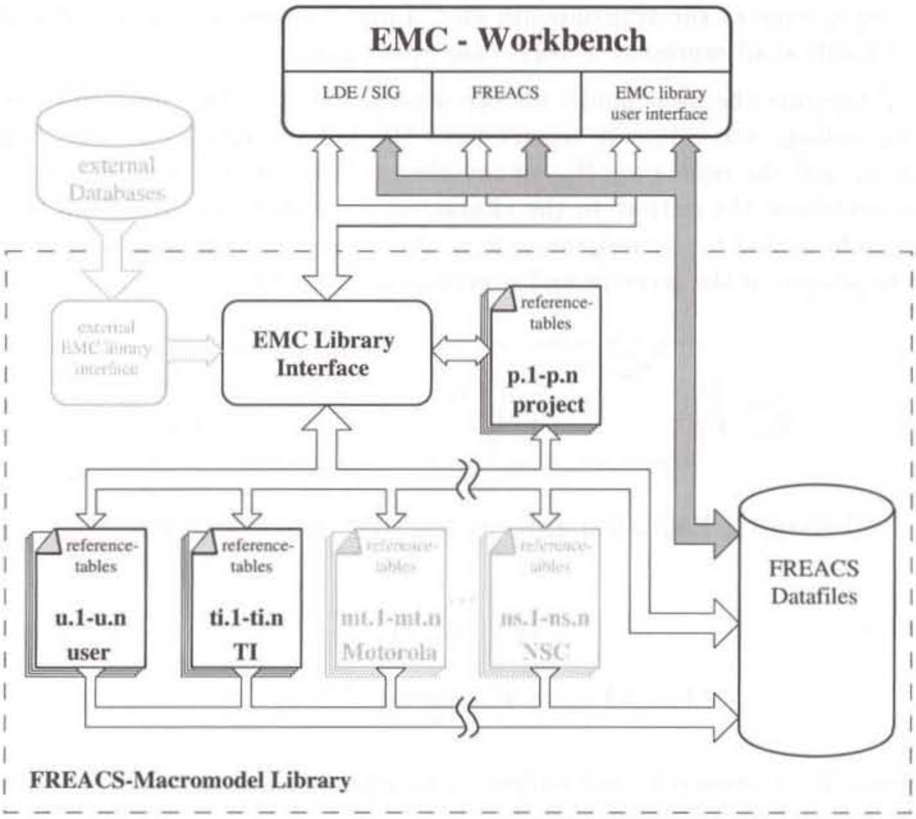

Figure 16: Prototype of the FREACS Macro-Model Library

To examine the preliminary concept of the EMC library structure a prototype which connects the FREACS macro-model library with the EMC–Workbench has been implemented

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as shown in Figure 16. For this purpose, the necessary reference tables, a basic library and a basic user interface have been developed. Currently, the library prototype is based on reference tables including standard logic components. Prototypes of the basic library and the user interface enables the user to interactively associate FREACS macro-models to digital components. The capability to create and modify user and project reference tables is also provided. Additionally, simple FREACS macro-models (model type 2) can be defined, stored and referenced.

6.2.1.2 LDE/LDA: Fast Pre-analysis Method

Increasing demands on circuits and PCBs result in faster component technologies, increasing clock rates, and PCBs with a higher complexity. Therefore, the design of PCBs has to be supported by fast analysis methods to avoid EMC effects in the early design phases, otherwise EMC effects like reflection and crosstalk may occur. Aim of the described pre-analysis is an approximate determination of the maximal voltage overshoot for a two-point-net without a time consuming simulation. Two-point-net means a layout structure consisting of one direct connection between two active components. It may contain passive components and the connection may consist of sections with different characteristic impedances. The reflection behaviour of digital circuits depends on the matching of the transmitter and receiver to the characteristic impedance of the transmission line. The reflection coefficients are effected by discontinuities of the characteristic impedance, and the propagation time of the transmission line. First principle of the introduced method is, that the result shall represent a worst case investigation.

Figure 17 presents the used model for the determination of the amplitudes of the first propagating voltage wave V_1. It results from the voltage divider of the characteristic impedance Z_L and the resistance R_{out} of the ideal voltage source. If a series resistance R_s is used for matching the output to the characteristic impedance Z_L of the transmission line, it has to be added to the resistance R_{out}. At the receiver the termination is given by the input resistance of the receiver and if necessary by matching measures.

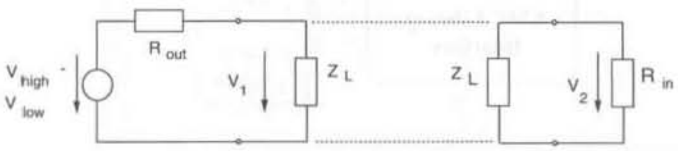

Figure 17: Equivalent Circuits for Transmitters and Receivers

$$V_2 = \rho(r) \cdot V_1 \tag{1}$$

$$V_1 = (V_{high} - V_{low}) \frac{Z_L}{R_{out,low/high} + Z_L} \tag{2}$$

As for most IC-technologies the output resistance of high/low transitions differ from that of low/high transitions, both cases have to be investigated separately. The procedure is described as exemplification for a low/high transition. $\rho(r)$ is a characteristic function describing the reflection behaviour of transmission lines.

Most PCBs have more than one signal layer. Therefore, many transmission lines will extend over more than one layer. A discontinuity of the characteristic impedance has to be

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expected at the via. Compared to the maximum overshoot of a homogeneous transmission line this case yields to a larger one. Figure 18 shows the ringing at the termination of a long transmission line for three different arrangements. The lengths of the line sections were chosen in a way that the amplitude is independent from the rise–time and the transmission line length itself.

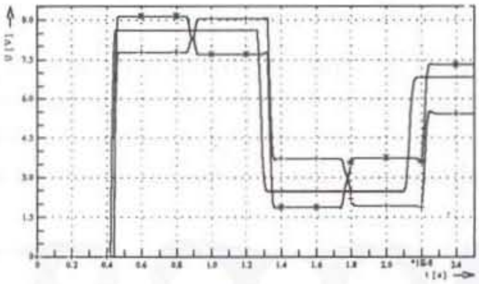

Figure 18: Voltage Ringing of a Long Line Without (–) and With a Layer Change (∗), (+)

Now it can be shown, that for a 'worst case' approximation the function $\rho(r)$ can be determined for N arbitrarily arranged characteristic impedance discontinuities as follows ($N+1$ homogeneous areas):

$$\rho = (1 + r_{in}) \prod_{i=1}^{N} (1 + r_i), \qquad r_i = \left| \frac{Z_{L(i+1)} - Z_{Li}}{Z_{L(i+1)} + Z_{Li}} \right|, \quad r_{in} = \left| \frac{R_{in} - Z_{L(N+1)}}{Z_{L(N+1)} + R_{in}} \right|. \quad (3)$$

The voltage, determined in equation (1), does not consider the influence of the line length (Figure 19).

The calculated maximum voltage amplitude is only valid for $2t_d \geq t_r$ (t_d: propagation delay of the transmission line, t_r: rise time of the digital signal). The approximated voltage has to be multiplied with the term $2t_d/t_r$ for shorter transmission lines. Considering the practically important mixed resistive/capacitive terminations, exponential curve-shape occurs.

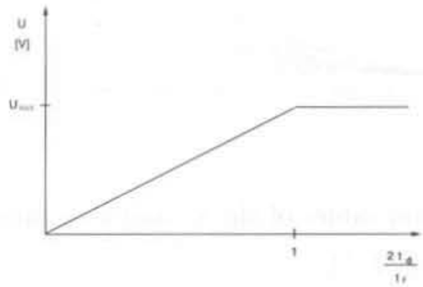

Figure 19: Voltage Amplitude of the Overshoot versus $2t_d/t_r$

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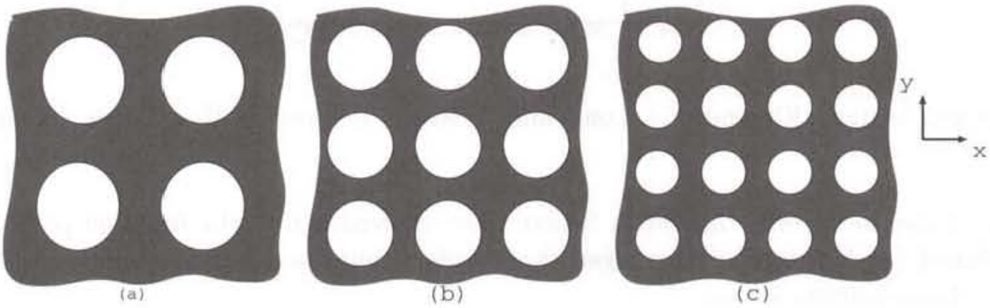
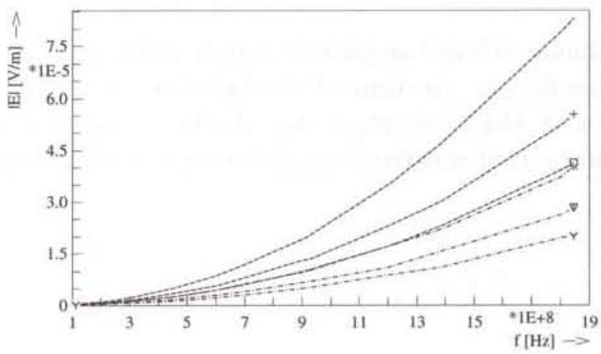
6.2.1.3 Application of the EMC–Workbench for the Analysis of High-speed–Systems

In the current report period, different application projects in the SNI development departments were supported. In addition to the analysis of printed circuit boards with respect to reflection and crosstalk effects, one project dealt with the analysis of apertures in system cabinets with respect to radiation effects. The rationale for this project was the necessity of minimising the radiation of a system by optimising the apertures.

As an example the analysis of an array of circular apertures is presented. The apertures were arranged in a conducting surface. On one side of the surface (inside housing) a plane wave was adopted. On the other side (outside housing) the electric field strength was calculated. With this model the shielding of housings has been analysed.



The analysis was performed for four different configurations. The total area of all apertures was held constant. The maximum of the electric field strength was compared.



The picture shows maximum values of the x– and z–component of the electric field:

4 apertures : {- - -: $|E_x|$, $*$: $|E_z|$}
9 apertures: {+: $|E_x|$, ∇: $|E_z|$}
16 apertures: {$\square$:$|E_x|$, y: $|E_z|$}

It is obvious that the radiation can be reduced significantly by varying the configuration although the total area does not change. The best results were obtained with configuration (c).

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6.2.2 Industrialisation of the EMC–Workbench

During the current report period, the industrialisation of the EMC–Workbench was pushed and a beta–release of the software has been completed. The corresponding release 1.2 consists of the tools

- MANDI (placement analysis),
- LDE/LDA (layout data extraction/layout data analysis),
- TALC (calculation of transmission line parameters),
- FREACS (simulation of reflection and crosstalk effects),
- SIG (generation of simulator input),
- EXLIN (extended library interface), and
- AnaRes (graphical post-processing).

All tools are integrated using the framework SIFRAME.

The software was presented at different exhibitions like CeBit '93 in Hannover, Design Automation Conference (DAC '93) in Dallas, and EURODAC '93 in Hamburg to evaluate the market for EMC–tools. Many contacts to potential users were established and feedback for further development activities was achieved.

6.2.3 Microsystem–Workbench

Cadlab's concept of a Microsystem–Workbench applies established paradigms of design-environment based design methodologies to the domain of micro-systems.

A micro-system contains different elements of different scopes like micro-mechanics, microelectronics, microfluiddynamics, micro-optics or micro-acoustics. There are several tools for every scope to support the development of the different elements and there are also some tools that work on the systems level. These tools generate data that describe some properties of the system. There could be a connection between some tools via the input and output files, i.e. the output file of one tool is the input file for another tool. This causes a very complex structure of data and interfaces.

To support the designer in calling the tools and managing the data a development environment has been built. For the implementation of the environment a framework was used with an object-oriented database. The integration of the tools into an environment helps to make the development process faster and safer. The integration reduces operating time between the use of different tools. Data management, like backup, versioning or commitment, requires time and great attention and is therefore a potential source of error. Beside data management, the environment helps to call the tools at the right time with the right parameters and with all needed input files.

There are different requirements to the list of tools that should be integrated into a development environment. There are so many tools that can be used alternatively, that it doesn't make sense to integrate all tools which are available for the development of

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micro-systems. To simplify the generation of different domain specific development environments a *generalised development environment* is created, that can be configured for special requirements. The starting point for the creation of the generalised development environment is a *generalised development process*.

The development flow of arbitrary systems has some characteristic features. These features are the basis for the generalised development environment. A complex system is divided into subsystems which itself could also be divided into subsystems, until a manageable *system hierarchy* has been constructed. The system and also the subsystems within the system hierarchy are developed in the same sequence of operational steps. So the development process can be divided into successive *development phases*. The third feature of a development flow is an *optimisation process*. If the developed system doesn't meet the requirements, the system will be optimised, i.e., some operational steps will be repeated, until an optimal solution is found.

The generalised development process serves as a model for the implementation of the development environment. The desktop of the environment shows the system hierarchy and the phases of the development process. For optimising the design, it must be possible to repeat phases in cycles.

The basis of the development environment is a *generalised object schema*. This schema defines the data structure of the database in an abstract manner. A schema for data that is generated during the development process, for example input data and output data of tools, is not yet determined. This will be an important task in the case of white-box integration of tools. The generalised schema is tightly coupled to the generalised development process. By employing appropriate object types it may be possible to build the system hierarchy like a tree. For this purpose, a so called entry object is created for the system and for each subsystem. This object serves as the entry to the development process of the corresponding system or subsystem. Data is further structured according to the phases of the development process. Entry objects for the phases are related to the system and each subsystem.

The generalised object schema is designed in a way that facilitates changes. Methods are defined for every phase. They represent activities that are performed during the phases. In the development environment the selection of a method shall start the execution of a tool.

In different domains like micro-electronics or micro-mechanics different tools are used in the development process. The above mentioned generalised object schema needs to be tuned to the domain correspondingly. The required tools are associated with the development phases. A micro-system contains usually subsystems that belong to different domains. For that reason different development environments, that are configured for special domains are integrated in a common environment.

6.2.4 Macro-Modelling of Analog Components

The analysis of noise behaviour of mixed analog/digital circuits becomes more and more important. To allow fast analysis macro-models for analog components considering parasitic effects are developed at Cadlab.

During the report period new macro-models for analog circuits were developed and different modelling approaches were analysed. The development of circuit models mainly

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depends on three aspects. First of all, the models must be usable for the available simulators. Secondly, the modelling is limited by the simulators input language. Last but not least different modelling strategies are possible.

The new macro-models are based on the block–oriented modelling approach[9]. This approach has the advantage that every model is composed of different stages, which can be reused within other applications. The stages are modelled structure–incompatible. Therefore, the existing models are technology–independent and provide a wide application range.

In Cadlab simulators with different input languages and modelling features are available. The mainly used simulators for analog applications are SPICE2G6[10] with netlist description language and ELDO[11] with behavioural and netlist description language. Therefore, macro-models for SPICE syntax and behavioural description were developed.

Each of the different languages has its advantages. Whereas the SPICE syntax is a simple and fast way of specification, the behavioural language leads to a high abstraction level, which can reduce simulation time.

To identify the influence of the used simulators and their description language a comparison was made between macro-models of an operational amplifier and a comparator, written in SPICE and FAS syntax. The macro-model of an operational amplifier was generated for the simulator SPICE and was transfered into the behavioural language FAS. This example was used to investigate any advantages in changing the description language but maintaining the model structure. In a second project a macro-model was written in SPICE syntax and independent from the SPICE model a behavioural model in FAS has been developed.

The operational amplifier models were simulated as a backtracked inverting operational amplifier with a gain of three. Figure 20 presents the simulation results.

As expected, the same results for both models were achieved. A comparison of the consumed simulation time shows that the time consumption for both models is nearly equal.

Fig. 21 shows the simulation results of two comparator models. The output behaviour of both models is nearly identical.

6.3 Summary and Outlook

During the report period, considerable progress has been achieved by the Analog System Engineering project group at Cadlab in the context of its EMC activities. For example a fast pre-analysis method regarding reflection effects was included in the EMC–Workbench. Also an EMC–library which contains macro-models for digital components was implemented.

The industrialisation of the EMC–Workbench was forced and a beta–release has been completed. All the different tools are integrated in the framework SIFRAME.

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[9] W. John and H.-T. Mammen: "Makromodellierung von einfachen und komplexen analogen Funktionselementen". Gesellschaft fuer Mathematik und Datenverarbeitung mbH, 5. E.I.S.-Workshop, 1991

[10] L. W. Nagel: "SPICE 2, A simulation program with integrated emphasis". ERL Memo ERL-M520, University of California, Berkeley (May), 1975

[11] ANACAD; "ELDO, Electrical Circuit Simulator". Version 4.1.x, ANACAD Computer Systems, 1993

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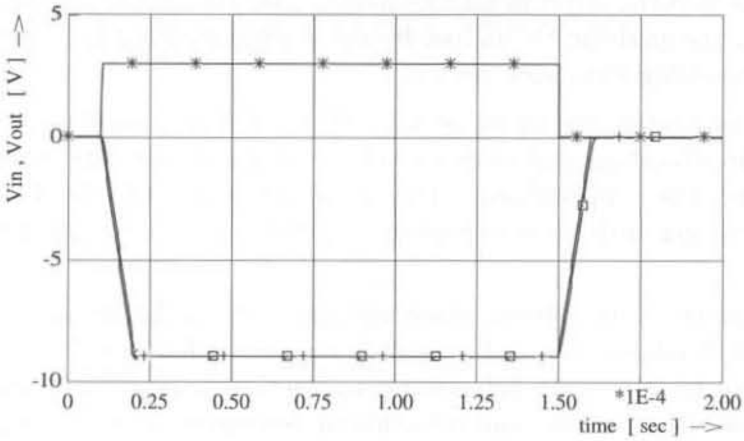

Input voltage : $\star$; Output voltage : FAS ($\square$), SPICE (+)

Figure 20: Transient Analysis of Operational Amplifier Model

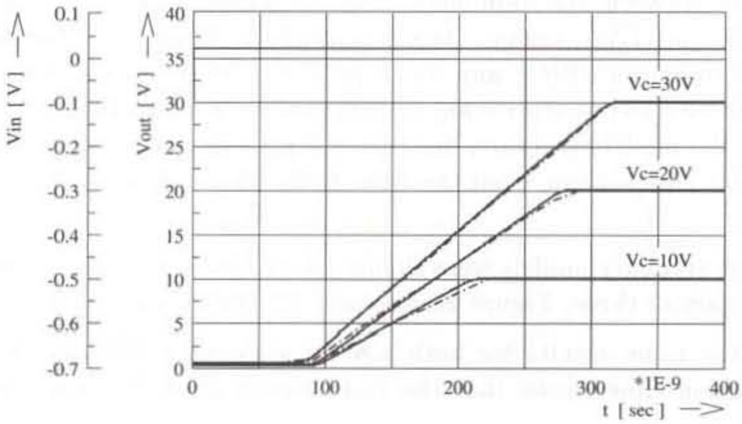

Figure 21: Transient Analysis of the Comparator Model

Furthermore, macro-models of analog components which are necessary for a fast and accurate simulation of analog circuits were developed.

To generalise the design process for arbitrary systems a prototype of a Microsystem–Workbench was developed. Tools of different domains like micro-electronics and micro-mechanics can be integrated.

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7 Technical Management Group and Computing Center

7.1 Baseline

Apart from the already existing group "Computing Center" another group, offering general services to all Cadlab teams, called "Technical Management Group, TMG" has been founded by January 1st, 1993.

Main objective of this new group during the report period has been the provision of support for "kicking off" Cadlab's efforts in the area of "Computer-Aided Concurrent Engineering, CACE".

From a technical point of view central focus of attention has been the evaluation and preparation of scientific material, the establishment and maintenance of external contacts as well as the internal coordination of Cadlab's R&D processes. Driving force of all these activities has been the request for creating an appropriate environment for the introduction and implementation of Cadlab's leading theme CACE in its administrative and technical aspects according to the pre-supposed planning horizon (about three to five years).

Another central topic have been measures for assuring that Cadlab's software development projects and their envisaged results satisfy the required quality criteria in order to facilitate the transfer of Cadlab's R&D work into SNI products. The framework for these quality criteria is given by SNI's quality principles, expressed in the SNI Process Handbook for Application Software, its Cadlab specific supplements and the ISO standard for quality assurance systems.

In addition, TMG had to deal with

- internal and external promotion and presentation of Cadlab and of its results;
- support and consultancy for the acquisition and management of international, collaborative projects;
- analysis of the CACE problem space in practice (CACE requirements engineering).

All these technical TMG activities have been complemented by a number of administrative coordination efforts, which included budget-controlling and commercial support of running and new Cadlab projects, and processing of all contractual issues. In addition, TMG has acted as interface to the relevant departments within SNI and Paderborn University.

7.2 Work During the Report Period

7.2.1 CACE Requirements Engineering

Work in 1993 concentrated on the participation in a project of an SNI plant in Paderborn, manufacturing UNIX computers. Within a global CAI-restructuring effort of this plant, the objective of this project is to design a conceptual schema for component part data. Examples for components are integrated circuits, capacitors, printed circuit boards, screws, or cases. A conceptual schema describes information types associated with these

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components, like size, weight, unique identification number, supplier, programming information, etc. A strong motivation for Cadlab to participate in this project is to understand current data handling practice and especially what kind of problems have to be solved by future software solutions.

A special problem turned out to be very difficult to solve: which information types are currently in use? A new component data schema must contain at least these information types. The new schema should not contain information types which nobody needs, because this would require useless maintenance effort. The difficulty to state whether a given information type is currently in use or not, is due to the following reasons:

- information type definitions are distributed over the whole plant;
- users do not know what information types are used by their software tools;
- users are not able to tell, precisely and completely, what information types they need for their every-day work.

During the report period an analysis of "information types in use" has been performed, based on information exchange between main computing systems (about 20 systems). This resulted in a list of more than 200 component attributes, which should be contained in the new component data schema. Currently, this new data schema is under development. A CASE-tool, "Innovator", is used for documenting the conceptual schema in a structured entity-relationship model. This project is planned to be finished in 1994.

The results of this project for Cadlab are twofold: the understanding

- of how to re-engineer a conceptual schema for plant data, and
- of the associated problem space.

For a special, new software solution from Cadlab in this area, Database Federation (DBF), the plant has agreed to play the role of a pilot customer.

7.2.2 Software Engineering and Quality Assurance

One of the goals of the Technical Management Group is to ensure that Cadlab's software development projects meet industrial quality standards. Therefore in 1993 continuous effort was made to introduce the guidelines of the SNI Process Engineering Handbook to the ongoing projects in all Cadlab working groups. Care had to be taken to apply those guidelines in a manner adequate for the special requirements of Cadlab with its deep integration of research and development. The necessary adaptations are documented in the "Cadlab Handbook for Software Development Projects".

Five Cadlab projects were supported during 1993: "EMC Workbench", "Advanced Editing Systems", "Intelligent Framework Services", "Database Federation Services", and "EXPRESS/STEP Environment".

"EMC Workbench" was the most advanced project. The Technical Management Group provided the project leader with consultancy concerning detailed planning of the technical realization phase and performed reviews of the functional specifications and user manuals.

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All other projects started in 1993 with a problem analysis. The Technical Management Group played the role of the "technical controller" in those projects. According to the SNI Process Engineering Handbook the technical controller checks at milestones whether a project proceeds according to the predefined development process and that the required results are achieved. During the analysis phase the main task of the technical controller was to review the following types of documents: "Statement of Problem", "Initial Situation Analysis", and "User Requirements Specification".

Additionally, the Technical Management Group gave presentations concerning "ISO 9000 - A Standard for Quality Management Systems" and "Software Quality Function Deployment" for all Cadlab employees and held a lecture for new employees to make them familiar with the software development process within Cadlab.

7.2.3 CADLAB Promotion and Presentation

Besides presenting Cadlab at various opportunities (e.g., at the meeting of the Paderborn "Wirtschafsförderungsgesellschaft") TMG contributed to a number of external brochures with references to Cadlab, e.g., to

- Research Report '90-'93 of Paderborn University;
- Cadlab section in "ZIAM[12]" brochure;

Internally, TMG coordinated the production of

- Cadlab Annual Report '92;
- Cadlab Objectives Paper '92;
- Cadlab Handbook;
- Cadlab Standard CACE slides set.

In addition, TMG contributed to the analysis of Cadlab's documentation environment and produced a number of templates and forms for documentation and promotion/presentation purposes, e.g., for slides and project documentation.

7.2.4 Project Acquisition and Coordination

During the report period, the CEC issued the second call of ESPRIT III and a number of proposals have been written with Cadlab participation. Both from administrative/organisational and technical points of view TMG gave support for the production of the following project proposals:

- DAISY, ESIP, KISSME and SYMMETRY (in cooperation with project group SET)
- FastEMC and EMAC (in cooperation with project group ASE)

[12]Zentrum für Industrielle Anwendungen Massiver Parallelität GMBH

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- ADVANCE and EMAC (as consultancy to SNI's BU ES CE division)
- ASSET Phase II

For the ADVANCE project further consultancy was provided during the production of the Technical Annex and for "kicking-off" the project at the end of the report period.

TMG also contributed to the specification of the ASSET Phase I Technical Annex in general and to its Task D3 "Framework Components" sections in particular. From the beginning of ASSET Phase I, TMG then coordinated this Task, which included the task's day-to-day management (progress and effort reporting, milestones tracing, etc) and the organisation of D3 meetings and workshops. In addition, the association of further D3 partners (Trinity College Dublin, University of Siegen, SSE Dublin) and negotiation of their contributions and contracts have been organised by TMG. A TMG representative attended several meetings of higher ASSET management bodies.

Administrative consultancy has been given to SNI SU AP 44 in the context of the ITHACA project and to Cadlab SET for the SYDIS project. In conjunction with the JCF Project Office the organisation of Cadlab resources in the JCF project have been coordinated.

7.2.5 Computing Center

The main task of the Computing Center group is the support and maintenance of an efficient programming environment for all Cadlab employees. This particularly includes the assistance of the employees and student assistants, the acquisition and installation of additional hardware and software tools, the improvement of the existing network and the task to keep all systems operational.

Furthermore the group Computing Center assists a group of Cadlab's industrial partner, SNI, which was part of Cadlab's former super project group "Framework" until October 1, 1992. These employees have their offices in the same building and use the same programming environment as all Cadlab employees.

7.2.5.1 Acquisition of Systems and Modules

The existing hardware equipment, mainly Sun and Silicon Graphics workstations, was expanded with additional workstations and Personal Computers. In order to supply a sufficient number of workstations and computing power for the growing number of employees and student assistants some Sun workstations were acquired and other Sun workstations were expanded with local disk capacity and memory. About 20 Personal Computers were acquired for management tasks, as replacement for an obsolete SNI proprietary system at the secretary's office and for software development. Depending on the special purposes the configurations of the Personal Computers range from Notebooks to Desktops to high-performance tower systems.

In order to backup roughly 100 GBytes of data each week a second so-called jukebox which changes up to ten tapes automatically was acquired. Additional licences of the software tool for the administration and realization of the backups were also necessary.

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7.2.5.2 Networking

Via a Sun workstation configured as a gateway, the local area network at Cadlab is part of the network at Paderborn University. Due to the installed permanent link it is possible to exchange electronic mail and data directly and to work interactively on computers at the university with acceptable performance. It also offers the entry to other networks worldwide.

Caused by the close co-operation with SNI/Munich it was necessary to get a more powerful connection than electronic mail to SNI. During the report period the temporary solution to exchange data with one computer at Munich using the existing connection into the Packet-Switching Data Network (Datex-P) of the Deutsche Bundespost Telekom was replaced. A permanent link to the SNI worldwide network offers now the necessary functions and sufficient performance needed for an efficient co-operation with SNI. The access to the SNI network is restricted, but the configuration of this new link can be expanded to reach other departments at SNI as well.

Since the beginning of 1993, the ground floor in the building is used in addition to the former floor for Cadlab. To minimise the costs for the necessary extension of the network the existing local area network was used. Via a bridge both parts of the network were connected. Due to the installation of additional workstations and Personal Computers a further partitioning of the network into subnets was necessary to minimise traffic load on single segments. Furthermore some changes to the configurations of the Sun workstations which are used as servers for diskless clients, local and licenced software etc. were done. At least one server was attached to each subnet to improve network performance.

7.2.5.3 Operating System Software and Tools

One of the main tasks of the Computing Center group is to build up and preserve a homogeneous programming environment which, at best, is available on all different hardware respectively operating systems' platforms.

With the support of some employees representing the other project groups at Cadlab the installation of locally used tools like TEX, printer spooler, gnu tools etc. was improved.

Some Sun workstations were installed with the new operating system Solaris to gain first experiences. Therefore the installation of locally used tools for Solaris was necessary. A general change to Solaris is not planned yet.

Depending on special purposes Personal Computers were acquired for different applications like software development tools, office automation software etc. As a first approach all Personal Computers were connected to the local area network at Cadlab with PC/NFS. A concept to support such a heterogeneous environment which consists of Personal Computers and different Unix workstations will be necessary.

7.2.5.4 Outlook

In the beginning of 1994, the reduction of obsolete hardware (SNI Targon /35) and corresponding peripheral devices will be organised.

The planning of a move to a new building for Cadlab will be continued. The Computing Center group is involved to plan the extension of the hardware and software equipment, a state of the art local area network and the connections to wide area networks.

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7.3 Summary and Outlook

One of the major achievements of TMG during the report period has been the establishment of TMG as new staff group within Cadlab, which was a bit difficult but also challenging due to the mutually orthogonal responsibilities of its members. Together with Computing Center a number of successful endeavours jointly performed with other Cadlab teams and SNI BU ES CE contributed to the fact, that TMG has emerged as a well-accepted organisation both within Cadlab and externally:

- industrialisation of the EMC workbench: software engineering and quality assurance consultancy of TMG contributed to keep the B70 deadline of this project still in 1993;
- acquisition and coordination of projects:
  - in cooperation with SNI BU ES CE the proposal for the ADVANCE project succeeded the difficult evaluation process of the CEC in the context of the 2nd call within ESPRIT III; in addition, by contributing to the production of the ADVANCE Technical Annex to be done within only some weeks, the project succeeded to get a contract from the CEC still in 1993;
  - in cooperation with SNI SU AP and Sietec Berlin the continuity in administering the ITHACA project was ensured;
  - in the context of ASSET the specification of the corresponding sections in the ASSET Phase I Technical Annex and "ramping up" of the Task D3 "Framework Components" under difficult conditions has been successfully performed;
- cooperation JCF: provision of SIFRAME 2.1 Online Help with SNI BU ES CE;
- administration: transfer of the administration of all contractual issues for Cadlab student assistants to TMG both for SNI and University ones has been finished;
- publishing and presenting the results of Cadlab's work in the CAI project in various manners;
- analysis of and proposals for improving Cadlab's documentation environment.

For 1994 TMG (for Computing Center see Section 7.2.5.4) will have to continue

- with the acquisition and coordination of projects;
- with CACE requirements engineering in the context of the CAI and JCF projects and with continuing to internally present and externally publish these results;
- supporting Cadlab teams in the area of software engineering and quality assurance;
- with the permanent improvement of Cadlab processes in the area of business administration and controlling.

Another topic for TMG will be the support for the organisation and realisation of the (forthcoming) move of Cadlab to its new premises.

However, major changes are expected in 1994 for TMG as a group as such because of the merger of Cadlab's SET and BT groups and the envisaged personal involvement of TMG members in this(/these) new group(s) and its projects.

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Part III

Publications, Funded Projects, and Scientific Collaborations

8 Publications and Major Documents

8.1 Cadlab External Reports

- "The Extended Symbolic Link Revision Control System EXSRCS", D. Zimmer, D. Nolte, G. Waßmuth (Cadlab Report 01/93)
- obTIOS: "A CAx-Framework Service for Building Concurrent Engineering Environments", R. Quester (Cadlab Report 02/93)
- "A formal model for coupling computer based systems and physical systems", M. Brielmann, B. Kleinjohann (Cadlab Report 03/93)
- "Ein einheitliches formales Modell zur Schnittstellenspezifikation und Hardwarebeschreibung", B. Kleinjohann, R. Milczewski (Cadlab Report 04/93)
- "Federated Database Systems - An Introduction -", E. Radeke (Cadlab Report 05/93)
- "Tight Integration and Synchronization of Distributed Graphical Applications", W. Müller, B. Kleinjohann (Cadlab Report 06/93)
- "Description of Timing Problems Using Petri Nets for Level-Independent Timing Verification", P. Altenbernd, R. Milczewski (Cadlab Report 07/93)
- "Lastbalancierung in einem parallelen Waveform-Relaxationsalgorithmus" H. Holzheuer, W. Rissiek (Cadlab Report 08/93)
- "Report on a Concept to Characterize Analog Components with Respect to their EMC Behaviour", D. Wagenblaßt (Cadlab Report 09/93)
- "Konzept zur blockorientierten Modellierung analoger Bauelemente", H.-T. Mammen, M. Schäder (Cadlab Report 10/93)
- "SULTAN Standard Universal Layoutinformation Transport Language", H. Woizeschke (Cadlab Report 11/93)
- "Cadlab Annual Report 1992", F.J. Rammig, B. Steinmüller (Cadlab Report 12/93)
- "System Level Design", F.J. Rammig (Cadlab Report 13/93)
- "Entwicklung eines strukturfremden Makromodells für den Blinkgeber U643B", H.T. Mammen, V. Geneiß, M. Schäder (Cadlab Report 14/93)
- "Report on a Method for Extraction of Layout Data on Board Level with Respect to the Requirements for EMC Verification", D. Wagenblaßt (Cadlab Report 15/93)
- "SYBES - A Language for Parameter Description", W. Thronicke (Cadlab Report 16/93)
- "Approaching the Denotational Semantics of Behavioral VHDL Descriptions", W. Müller (Cadlab Report 17/93)

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- "Flexible Unterstützung kooperativer Entwurfsumgebungen durch einen Transaktions-Baukasten", A. Meckenstock, R. Unland, D. Zimmer (Cadlab Report 18/93)
- "Ein Framework für die parallele Validierung von STEP-Produktdaten", G. Lehrenfeld, W. Müller, N. Wiechers (Cadlab Report 19/93)
- "Express-P - Eine Erweiterung von ISO 10303-11 zur Prozeßmodellierung", W. Felser, W. Müller (Cadlab Report 20/93)
- "JESSI-Common-Framework JCF - An Open Framework for Integrated CAx-Environments", B. Steinmüller (Cadlab Report 21/93)
- "Vom Schema zur Sicht: Änderungsmöglichkeiten bei der Sichtableitung in einem objektorientierten Datenbanksystem", W. Heijenga (Cadlab Report 22/93)
- "FADE: A Layout Facility for Graphed-based Diagrams", H.J. Eikerling, W. Müller (Cadlab Report 23/93)
- "Development of an Analytical Approach to B-Spline-Functions of Second and Third Order for MOM Applications", S. Öing, W. John, G. Mrozynski (Cadlab Report 24/93)
- "Zur Makromodellierung von digitalen Bauelementen", W. John, O. Rethmeier (Cadlab Report 25/93)
- "Transactionrecovery in Entwurfsumgebungen", A. Meckenstock (Cadlab Report 26/93)
- "Regelmechanismen für Entwurfsumgebungen", D. Zimmer (Cadlab Report 27/93)
- "Introduction to Database Federation Services", E. Radeke, D. Nolte, S. Kolmschlag, G. Kachel (Cadlab Report 28/93)
- "Verfahren zur Berechnung der charakteristischen Parameter von Verdrahtungsstrukturen auf Leiterplatten und Mikrowellenschaltungen", W. John, U. Gierth, R. Remmert, M. Vogt (Cadlab Report 29/93)
- "Das ISF-Datenschema", J. Becker, F. Buijs (Cadlab Report 30/93)

8.2 Cadlab Internal Reports

- "Vergleich zwischen Motif und InterViews", H.-J. Kaufmann (Internal Report 01/93)
- "Beschreibung eines Bibliothek-Konzeptes für analoge und gemischt analog/digitale integrierte Schaltkreise", D. Wagenblaßt (Internal Report 02/93)
- "Products and Prototypes of Federated Database Systems", E. Radeke (Internal Report 03/93)
- "Cadlab Ziele, Grundaufträge und Aufgabenbeschreibungen (Version 1.0)", F.-J. Stewing (Internal Report 04/93)
- "Das Cadlab Handbuch", J. Strauß (Internal Report 05/93)
- "EXSRCS The Extended Symbolic Revision Control System", D. Nolte (Internal Report 06/93)

8.3 Major Software Documents

- EMC-WORKBENCH V1.2, Administrationshandbuch

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- SULTAN V1.3.3, Formatbeschreibung
- LDE V1.0, Benutzerhandbuch
- AnaRes – Analyse Results, Benutzerhandbuch
- TALC – Transmission Line Calculator, Benutzerhandbuch
- FREACS – Fast REflection And Crosstalk Simulator, Benutzerhandbuch
- FREACS – Makromodelle, Benutzerhandbuch
- ManDi – Manhattan Distance, Benutzerhandbuch
- "Studie der Integrationsoptionen EXPRESS/GRAPES", S. Bublitz (Cadlab), Heyes (EMSC), January '93
- "Testbericht zum DECexpress Editor", S. Bublitz, W. Müller, J. Strauß, March '93
- "Testbericht zum EXEP System", S. Bublitz, F. Buijs, W. Müller, J. Strauß, March '93
- "JCF SP4 Evaluation Report, JCF R2.0/2.1, JCF/ICL/011-01", (CoAuthors M. Brielmann, R. Milczewski, J. Stroop), May '93
- "HIS (High Level Interface System) - Delta Description to SLANG 1.0 -", W. Heijenga, B. Burkert, Y. Engel, G. Kachel, May '93
- "Entire 3.1.1 - Installation und Benutzung", R. Boettger, August '93
- "Statement of Problem - Database Federation Services", E. Radeke, D. Nolte, G. Kachel, August '93
- "Das Data Dictionary Schema für SLANG1.0", B. Burkert, Y. Engel, W. Heijenga, G. Kachel, August '93
- "Initial Situation Analysis - Database Federation Services", Y. Engel, G. Kachel, D. Nolte, E. Radeke, September '93
- "Manual-Pages für ExSRCS (Extended Symbolic Revision Control System)", D. Nolte, October '93
- "EXE.1/A30.3/2 — EXPREME", S. Bublitz, H.-J. Kaufmann, November '93
- "Problem Space Specification - Database Federation Services", R. Böttger, Y. Engel, G. Kachel, S. Kolmschlag, D. Nolte, November 93
- "EXE.1/A30.3/1 — EXPREME", S. Bublitz, F. Buijs, December '93

8.4 Books, Conference and Journal Papers

- P. Altenbernd, R. Milczewski: "Description of Timing Problems Using Petri Nets for Level-Independent Timing Verification", Proceedings of ACM/SIGDA Workshop on "Timing Issues in the Specification and Synthesis of Digital Systems", TAU, Malente, 1993
- P. Altenbernd, R. Milczewski: "Using Petri Nets for the Description of Timing Problems in Level-Independent Timing Verification", Proceedings of the Workshop on "Power and Timing Modeling for Performance of Integrated Circuits", PATMOS, La Grande Motte, 1993, pp. 101-112

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- M. Brielmann, B. Kleinjohann: "Petri Nets as a Common Model for Combined Physical and Computer Based Systems", Proceedings of the GI Workshop on "Petri-Netze im Einsatz für Entwurf und Entwicklung von Informationssystemen", Berlin, 1993, pp. 114-126
- M. Brielmann, B. Kleinjohann: "A formal model for coupling computer based systems and physical systems", Proceedings of the European Design Automation Conference, Euro-DAC, Hamburg, 1993, pp. 158-163
- F. Buijs, R. Selent: "Automatische Generierung von Datenpfad-Layouts", Proceedings of the 6. E.I.S.-Workshop, Tübingen, 1993, pp. 218-222
- E. Griese, J. Schrage: "Schnelle Berechnung von Reflexions– und Crosstalkeffekten auf gekoppelten Leitungssystemen komplexer Leiterplatten", Kleinheubacher Berichte 1993, Darmstadt, 1994.
- M. Holena: "Choice of Neural Network Architecture Using Lattice Theory", Proceedings of ISANN93 – 1993 International Symposium on Artificial Neural Networks Hsinchu, Taiwan, December 1993
- M. Holena: "Ordering of Neural Network Architectures", Neural Network World, 3, 1993, pp. 131-160
- W. John: "Komponenten- und Systementwurf unter EMV-Gesichtspunkten", Kleinheubacher Berichte 1993, Darmstadt, 1994.
- W. John: "Support of Printed Circuit Board Design by an EMC–Workbench", Proceedings of the 10th International Zurich Symposium and Technical Exhibition on Electromagnetic Compatibility, Zurich, 1993, pp. 185–194
- W. John, U. Gierth, R. Remmert, M. Vogt: "Parametrisierung von Verdrahtungsstrukturen auf Leiterplatten und Mikrowellenschaltungen", Kleinheubacher Berichte 1993, Darmstadt, 1994.
- W. John, E. Griese, J. Müller: "Entwicklung von Regeln für den Leiterplattenentwurf unter EMV–Gesichtspunkten", Kleinheubacher Berichte 1993, Darmstadt, 1994.
- W. John, D. Ley, F. Kruse: "Analyse von Reflexionen auf Leiterplatten durch einen wissensbasierten Ansatz", Kleinheubacher Berichte 1993, Darmstadt, 1994.
- W. John, J. Schrage: "Ein Konzept für den EMV-gerechten Mikrosystementwurf", Workshop "Informationstechnik für Mikrosysteme", Kernforschungszentrum Karlsruhe, 1/93
- W. John, H. Woizeschke, A. Hundsdörfer: "Layoutdatenextraktion f"ur den EMV-gerechten Leiterplattenentwurf", Kleinheubacher Berichte 1993, Darmstadt, 1994.
- B. Kleinjohann, R. Milczewski: "Ein einheitliches formales Modell zur Schnittstellenspezifikation und Hardwarebeschreibung", Proceedings of the GI/ITG Workshop on "Formale Methoden zum Entwurf korrekter Systeme", Bad Herrenalb, 1993, pp. 41-48
- H.-T. Mammen: "Entwicklung eines blockorientierten, strukturfremden Komparator-Makromodells ", Tagungsband zur 2. GME/ITG Diskussionssitzung "Entwicklung von Analogschaltungen mit CAE-Methoden", Ilmenau, 1993, pp. 186-192
- W. Müller: "Approaching the Denotational Semantics of Behavioral VHDL Descriptions", Proceedings of the 1st Asian Pacific Conference on Hardware Description Languages, Standards and Applications, Brisbane, 1993, pp. 141-145

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- W. Müller, B. Kleinjohann: "Tight Integration and Synchronization of Distributed Graphical Applications", Seventh Annual Database Symposium, ASME, San Diego, 1993, pp. 49-59
- W. Müller, G. Lehrenfeld, N. Wiechers: "Parallel Validation of STEP Files", Proceedings of the 3nd EXPRESS User's Group Conference, Berlin, 1993, pp. 147-157
- Stefan Öing, Gerd Mrozynski: "Elektromagnetische Kopplung und Strahlungsfeld von Leiterbahnen" Kleinheubacher Berichte 1993, Darmstadt, 1994.
- F.J. Rammig, U. Kastens, P. Pfahler, C. Nagel: "Design of a VLIW Architecture Constructed from RISC Chips: A Case Study of Hardware/Software Codesign", Proc. Euromicro '93, 1993.
- F.J. Rammig: "Modelling Aspects of Integrated System Design", Proc. EURO-DAC/EURO-VHDL '93, 1993.
- F.J. Rammig: "System Level Design", Mermet (ed.), Fundamentals and Standards in Hardware Description Languages, pp. 109–151, Kluwer, 1993.
- F.J. Rammig: "DACAPO III: A Retrospective", Mermet (ed.), Fundamentals and Standards in Hardware Description Languages, pp. 109–151, Kluwer, 1993.
- R. Remmert, W. John, E. Griese, M. Vogt: "Calculation of Transmission Line Parameters Using the Boundary Element Method", Digest of the International 1993 URSI Radio Science Meeting, University of Michigan at Ann Arbor, 1993
- R. Remmert, W. John, M. Vogt: "Calculation of Transmission Line Parameters Using the Boundary Element Method Based on an Adaptive Node Distribution", Record of the 9th COMPUMAG Conference on the Computation of Electromagnetic Fields, Miami, 1993, pp. 170–171
- W. Rissiek, H. Holzheuer: "Lastbalancierung in einem parallelen Waveform–Relaxationsalgorithmus", Tagungsband zur 2. GME/ITG Diskussionssitzung "Entwicklung von Analogschaltungen mit CAE–Methoden", Ilmenau, 1993, pp. 59–65
- B. Steinmüller: "JESSI-Common-Framework JCF – An Open Framework for Integrated CAx-Environments", Proc. 5th International Conference on HCI, Vol. 19A, p. 337ff, Orlando, Fl., Aug. 1993.
- W. Thronicke: "Anwendung einer Symbolbeschreibungssprache zur flexiblen Parametrisierung von analogen Makromodellen", Tagungsband zur 2. GME/ITG Diskussionssitzung "Entwicklung von Analogschaltungen mit CAE-Methoden", Ilmenau, 1993, pp. 174-179
- W. Thronike, H.–T. Mammen, R. Brüning, W. John, W. Rissiek: "Effiziente Makromodellierung analoger Bauelemente mit einer Werkzeugumgebung", Tagungsband zum 6. E.I.S.–Workshop "Entwurf Integrierter Schaltungen", Tübingen, 1993, pp. 384–394
- R. Zhao: "Gesture Specification and Structure Recognition in Handsketch-Based Diagram Editors", Proceedings of the 5th International Conference on Human-Computer Interaction, Orlando, 1993, pp. 1052-1057
- R. Zhao: "Handi: A Framework for Building Handsketch-Based Diagram Editors", Proceedings of the 5th International Conference on Human-Computer Interaction, Orlando, 1993

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- R. Zhao: "Handsketch-based Diagram Editing", Teubner-Texte zur Informatik Band 5, B.G. Teubner Stuttgart Leipzig, 1993
- R. Zhao: "Incremental Recognition in Gesture-Based and Syntax-Directed Diagram Editors", Proceedings of the ACM Conference on Human Factors in Computing Systems (InterCHI '93), Amsterdam, 1993, pp. 95-100

8.5 PhD Theses

The following PhD Thesis has been completed during the report period:

- Werner Rissiek: "Anwendung von Waveform–Relaxationsverfahren in der Schaltungssimulation", November 1993

8.6 Masters Theses

The following master theses have been completed at Paderborn University under the responsibility of Cadlab:

- A. Leventis: "Kreativer objektorientierter Entwurf: Prototyp eines Werkzeuges"
- Hamid Nait-Challal: "Berechnung der charakteristischen Parameter von Leiterbahnen in Multilayertechnik durch Lösung eines gemischten Randwertproblems"
- Michael Schäder: "Entwicklung eines Makromodells für Timer-Funktionselemente"
- Ralf Seepold, Thomas Wollny: "Eine Werkzeugumgebung zur Überwachung und Steuerung eines verteilten Datenbanksystems - DACS"

8.7 External Talks, Lectures, Tutorials, Panels

- S. Bublitz: "Express", CONSENS Workshop, Munich, May '93
- P. Drescher: "Intelligent Framework Services (IFS)", Poster at JCF SP1 Workshop, Spitzingsee, June '93
- F. Buijs: "Das Projekt EXPRESS/STEP Environment", SNI STEP User Group, Nürnberg, November '93
- S. Kolmschlag, D. Nolte, E. Radeke, F.-J. Stewing: "Heterogeneous Database Systems", Asset-Workshop, Task D3 "Framework Components", Subtask D3.4 "Evaluation of Heterogeneous Database Technology Migration", Paderborn, November '93
- E. Radeke: "C++ Tutorial", Paderborn University, June '93

8.8 Exhibitions

Cadlab results have been presented at the following exhibitions:

- CeBIT'93, Hannover, March '93
- EMC'93, Zürich, March '93
- EURODAC'93, Hamburg, September '93

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9 Funded Projects

9.1 Nationally Funded Projects

During the report period, Cadlab participated in a number of cooperation projects supported by the BMFT or AiF[13] as indicated in tables 11.1 and 11.2.

Title	Support program	Run time	Project partners
EMC-Design	BMFT	04.88 – 03.93	Bosch, TU–Berlin, FH Wiesbaden, Uni Stuttgart, TEMIC
MST-BIB	BMFT	04.91 – 04.95	ABB CEAG LuS, Uni-GH-Paderborn, Uni Bremen, Bosch, DOSIS, FH Wiesbaden, FhG-AIS, Hahn Meitner Institut, Krone, Rhode & Schwarz, SRM-CAE, TU Braunschweig, Uni Dortmund, Texas Instruments, Mikron
MST-MW	BMFT	7.92 – 12.96	KfK/IDT, FhG-IIS, GMD, MBB, Uni-GH Wuppertal, Siemens, FhG-IIS-EAS, SNI, BOTEC, ebm, ETA, Harting, Jenoptik, Kuhnke, Mannesmann Tally, MicroParts, PROFI Engineering, AST, VDO, TU Berlin, Bosch, TU Chemnitz, Uni Erlangen, Uni-GH Paderborn
MST-UEM	BMFT	06.92 – 05.94	KfK/IDT,FhG–IMT, UniBW München, GMD, Uni Erlangen, TH Ilmenau, TU Magdeburg, FH Augsburg, TU Chemnitz, TU Berlin, Uni Jena

Table 11.1: Nationally Funded Projects

[13] Arbeitsgemeinschaft industrieller Forschungsvereinigungen e.V.

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Title	Support program	Run time	Project partners
JESSI AC5	BMFT	07.92 – 06.95	ABB, Bull, DASA, GFAI, ITALTEL, MATRA, Mercedes–Benz AG, Philips, RFT–SEL, THESYS, TU Ilmenau, Vectorfields, Philips Research Labs (UK)
JESSI AC12	BMFT	01.92 – 12.92	ANACAD, Bosch, CSEM, EZM, FhG/EAS, MATRA, Philips, Siemens, SGS–Thompson, S3, TEMIC
OMSI	BMFT	08.91 – 12.94	Humboldt-Uni Berlin, TH Ilmenau, Uni-GH Pb
OPAL	AiF	12.92 – 05.94	GFAI, Parsytec
QUELLE	DtA	09.93 – 03.96	GFAI, Widis, Uni Paderborn, TU Danzig
SYDIS	BMFT	01.93 – 12.95	GMD, Uni-GH Paderborn, FhG-EAS, FZI Karlsruhe

Table 11.2: Nationally Funded Projects (Cont.)

9.2 European Funded Projects

In the report period Cadlab participated in the CEU funded projects (ESPRIT) as outlined by Table 11.3.

Title	Support program	Run time	Project partner
ESIP	ESPRIT–II/III	10.93 – 09.95	Bull, ICL, SNI, Siemens, Thomson-CSF, Racal-Redac, Philips (Univ–Paderborn assoc. to SNI)
JESSI-Common-Frame	ESPRIT–II	05.93 – 04.94	Project Leadership: SNI ICL, SGS-Th., Siemens, Philips, Racal-Redac, TU-Delft (Univ.–Paderborn assoc. to SNI)
ASSET I	ESPRIT-III	03.93 – 04.94	Bull, Olivetti, Philips, CAP Debis SSP, Emeraude, TCD, Uni Siegen, SSE, Sysdeco

Table 11.3: European Funded Projects

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9.3 Reports on Funded Projects

MST-UEM Reports:

- J. Schrage, M. Gutzmann, W. John: "Berücksichtigung von EMV-Problemen im Vorfeld von System- und Hardware-Architekturentscheidungen bei der Mikrosystementwicklung", Zwischenbericht, 2/93
- J. Schrage, W.John: "Ein Konzept zur durchgängigen Berücksichtigung der EMV beim Entwurf von Mikrosystemen", Statusbericht, 8/93

MST-BIB Reports:

- R. Brüning, H.-T. Mammen, W. Thronicke, W. John, W. Rissiek: "2. Zwischenbericht (Period 01/92-12/92)", March 1993
- R. Brüning, H.-T. Mammen, W. Thronicke, W. John, W. Rissiek: "3. Statusbericht (Period 15.10.92-15.10.93)", October 1993

JESSI AC5:

- "Technical Report (Period 01/93–06/93)", July 1993
- "Technical Report (Period 07/93–12/93)", December 1993

JESSI AC12:

- "Technical Report (Period 01/93–06/93)", July 1993
- "Technical Report (Period 07/93–12/93)", December 1993

OMSI Reports:

- E. Frank, F. Buijs, T. Lengauer, 3. Halbjahresbericht (01.08.92 – 31.01.93), February '93
- F. Buijs, E. Frank, T. Lengauer, 4. Halbjahresbericht (01.02.93 – 31.07.93), August '93

SYDIS Reports:

- S. Bublitz, J. Tacken, 1. Halbjahresbericht (01.01.93 – 30.06.93), July '93
- J. Becker, F. Buijs, "Das ISF-Datenschema", December '93

ECIP/ESIP Reports:

- Wolfgang Müller: "Eemir (Prototype) - User's Guide", (Deliverable RC:1.1.2.51.B - Row 8), ECIP2/PU/016-1, June '93
- Wolfgang Müller, Georg Lehrenfeld: "Validation of EXPRESS Models (Preliminary Report)", (Deliverable R:C1.6.2.51.B - Row 16), ECIP2/PU/017-1, June '93
- C. Oczko, Key Deliverable KD_C_2.1_51_p, "Modeling Rules for Mapping a Multi-Kernel Description to VHDL", Key Deliverable KD_C_2.1_51_p, June '93

ASSET Reports:

- S. Bublitz, Design of the EXPRESS-G Editor EXPREME, October '93
- Draft Asset-Report D.D3.4/1 "Problem Analysis and Requirement Specification on Heterogeneous Database Systems", R. Boettger, Y. Engel, G. Kachel, S. Kolmschlag, D. Nolte, E. Radeke, Dezember 1993

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JESSI-Common-Frame Reports:

- JCF/CADLAB/064-01/03-Nov-93 "Meta Schema for Hybrid Knowledge Representation and Management"
- JCF/Cadlab/065-01/02-Dec-93 "Theoretical Principles of Uncertainty Processing in Expert Systems"

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10 Collaboration in Technical-Scientific Bodies

GI/GME/ITG:

- Leadership of ITG Technical Committee 5.2 (CAD) (F.J. Rammig)
- Member of GI Technical Committee 3.5 (CAD) (F.J. Rammig, B. Steinmüller)
- Member of Steering Committee for Working Group GI 3.5.1/ITG 5.2.3 "Methods for the Design and Verification of Digital Circuits and Systems" (F.J. Rammig)
- Member of Steering Committee for Working Group GI 3.5.4/ITG 5.2.6 "CAD Umgebungen für den Entwurf mikroelektronischer Systeme" (B. Steinmüller, F.-J. Rammig)
- VDI/VDE-GME Technical Committee "Informationstechnik für Mikrosysteme" (W. John)
- Member of GI FG 4.2.1 AK 7 "Produktmodell / Datenmodellierung" (F. Buijs)
- Member of GI FG 2.5.1 "Datenbanken" (G. Kachel, E. Radeke)

IFIP:

- National representative for Germany in IFIP TC10 (F.J. Rammig)
- Member of IFIP WG 10.2 (F.J. Rammig)

CFI:

- CFI Inter-Tool Communication Working Group (M. Joosten)
- CFI Working Group Simulation Backplane (M. Niemeyer)

Others:

- Member of Steering Committee of VHDL-Forum for Europe (F. J. Rammig)
- CFI TSC Component Information Representation European Co-chair (W. John)
- VHDL Reballoting Group (C. Oczko, W. Müller)
- Balloting Member of IEEE Std 1076-1992, VHDL'92 (C. Oczko, W. Müller)
- Balloting Member of IEEE Std 1164-1993 "IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164)" (W. Müller)
- IEEE Taskforce on the Engineering of Computer-based Systems, ECBS (M. Brielmann, F.-J. Stewing)
- Member of CENELEC TC117 WG1 (W. Müller)

Program Comittees, Organization of Sessions at Conferences:

- Member Program Committee GI Annual Conference, Application Workshop, Dresden 1993 (B. Steinmüller, F. J. Rammig)