cadlab

Annual Report 1994

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Cadlab Annual Report

1994

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Preface

When in 1985 Cadlab, the joint R&D institute of Paderborn University and Siemens Nixdorf Informationssysteme AG was founded this was driven by the intent to bridge the traditional gap between academia and industry by deeply integrating university research and industrial development. While university research is mainly driven by the desire to increase knowledge, industry has to be pushed by the market. It was the basic idea of the founders of Cadlab to combine these two cultures as closely as possible in order to maximize cross-fertilization and to stimulate innovation. Thus, in this unique joint R&D institute "Cadlab" engineers and scientists, although hired from both sides, work together day by day under one roof, jointly search for innovative solutions in mixed project groups and share problems and visions. During nine years of collaborative work Cadlab has proven that its founders' ideas not just remained a dream but became reality.

Cadlab's objective is to advance the field of engineering of computer based systems and to provide its partners with sophisticated solutions for solving complex engineering problems. During the report period numerous publications, including seven dissertations, have demonstrated the scientific success of Cadlab, while its achievements in precompetitive product development have been demonstrated by a couple of development cycles that reached a state mature enough to be ready for industrial exploitation. The EMC-Workbench may serve as one of the most impressive examples. This solution for a demanding and fast growing market has been transferred to a newly created spin-off company, called INCASES Engineering GmbH. Due to Cadlab's unique organisation and a consequent path from applied research to user oriented development, INCASES can offer today one of the most advanced solutions worldwide in this area.

From the beginning Cadlab's work has been inspired by the vision of providing smoothly integrated environments to the user in order to optimise the overall engineering process instead of isolated tools. Consequently, in the past research and development on tools always included the aspect of building integrated tool sets or "workbenches". Driven by requirements of its industrial partner Cadlab invested a large amount of its manpower in the design and implementation of the JESSI Common Framework which emerged into SNI's SIFRAME product. After technology transfer to its industrial partner in 1992 and appearance of framework technology on the market, Cadlab shifted its focus to additional advanced techniques of framework technology and on demanding application areas. As examples the following areas may serve: development of an open database middleware toolkit, the support of knowledge based engineering techniques, the realization of an operating system independent advanced editing toolkit, modelling of heterogeneous systems, the above mentioned EMC-Workbench and information exchange via standardised formats (STEP/EXPRESS).

At the end of the report period, about 70 scientists and engineers, and more than 100 student assistants and students preparing their master's thesis were employed in Cadlab. They are organised in two main groups, dealing with "Information Technology" and "Analog System Engineering". In addition there is a "Technical Management Group and

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Computing Center". 10 employees moved to INCASES during the last quarter of the report period.

Cadlab's results during the report period will be discussed in more detail in the following sections of this report. Therefore only some highlights shall be summarised here.

In future the coexistence and federation of established databases will be of great importance. This is due to the fact that the huge amount of data which is stored in existing databases forms an enormous investment, which on the one hand needs to be preserved, while on the other hand much more coordinated, efficient access facilities are urgently needed. Furthermore, database indepence and migration are strong requests needing an answer. Cadlab developed a technology to solve this set of problems by providing a modular toolkit called "Open Database Middleware Open DM". This approach was developed towards the pilot stage during the report period.

Knowledge based techniques also made considerable progress in the last years. By means of its IFS project Cadlab will offer an environment that supports the integration of knowledge based techniques into engineering systems. The architecture follows the proposals of the IEEE working group P1252.

As advanced user interfaces become more and more the key point of any computerised applications, Cadlab invested into the design and development of an advanced, platform independent graphical editing system. During the report period a major part of this system, the Editor Operating System EOS, was driven through two version cycles and successfully used to build first applications.

As complex computer based systems tend to be heterogeneous, a unified modelling approach seems to be necessary for creating a joint basis. On the other hand the unwieldiness of a large uniform model as well as the desire of the users to keep their preferred data views must be respected. Therefore Cadlab developed an approach that allows the various users to stay in the modelling environment they are familiar with, while internally a unified modelling paradigm is provided, whereupon all external model parts needing unification can be mapped.

The communication of data is increasingly based on STEP protocols. To support this trend a STEP/EXPRESS workbench has been designed at Cadlab. This software, too, has reached product quality and has been licensed worldwide to interested organisations.

Last, but not the least, Cadlab's most complex software system transferred to the market in this report period is the EMC Workbench. It is one of the leading design environments worldwide to support the design of printed circuit boards under EMC constraints. The successful use of this software within various departments of SNI and Siemens demonstrated its quality and fundamental importance. At the same time research towards a workbench supporting system design under EMC constraints has been continued. This research area covered e.g. parallel high performance simulation, an EMC advisory system, and a macro modelling environment.

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Cadlab's standardisation efforts have been concentrated on active participation in various international bodies. Areas of Cadlab's standardisation contributions included VHDL, STEP and EXPRESS, Data Modelling, Simulation Backplanes, Object Oriented Databases, Engineering of Computer-Based Systems.

Cadlab's international scientific reputation is reflected by the large number of publications. Cadlab employees have presented papers on most major international conferences on topics related to Cadlab's focus of research. In addition, Cadlab members have been active in organisational bodies of such conferences.

1994 was a year that demonstrated the intent and ability of Cadlab to anticipate upcomming demands and interests of Cadlab's constituting partners as well as trends and developments of the international research and user community. By concentration on leading edge pre-competitive areas the workforce could be focused on future-oriented goals. On the other hand, Cadlab has kept its proven main principles: tight integration of academic research and industrial development and focus on application oriented research and development topics.

The following annual report gives an overview of Cadlab's activities and achievements in 1994. Part I of the report details Cadlab's objectives, describes Cadlab's organisational structure and gives a general overview of the progress made. Part II contains technical details from the project groups. Part III provides supplementary information on publications, funded projects, and cooperations.

F.J. Rammig and B. Steinmüller
Cadlab Executive Board
Paderborn, May 1995

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I Overview

1 Goals and Objectives

1.1 Principal Goals

Cadlab, the joint research and development institute of Paderborn University and Siemens Nixdorf Informationssysteme AG, SNI, has been founded in 1985 with the backing of the federal state of North-Rhine-Westphalia.

The vision behind this unique endeavour has ever since been to deeply integrate university research and industrial development within a joint centre of excellence for the synergetic benefit of the partners as well as the public.

The mission is to provide innovative computer-based solutions for challenging industrial problems and to support bi-directional technology and know-how transfer from academy to industry.

Cadlab's mission materializes in the following tangible R&D results:

- reports,
- publications and PhD theses,
- software prototypes,
- software components with industrial quality standard.

Moreover, it is Cadlab's objective to supply high-quality R&D services in the following areas

- consultancy,
- education and training,
- coordination and support of complex R&D projects.

1.2 Objectives of the Report Period

The objectives of this report period were determined by the new strategic R&D directions and work programmes defined in the recent report periods as well as the actual requirements and needs by Cadlab's partners and customers. In particular, key objectives were

- to consolidate the work organization in the area of information engineering
- to provide software pre-products and pilot software in the areas of data base federation, advanced editing systems, and product modelling

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- found a spin-off company for the commercialization of the key results achieved in the area of analog system engineering
- initiate a new work organization and new work topics in ASE

In view of the upcomming termination of several projects executed within the third framework programme of the European Union, the preparation for the forth European framework programme as well as for new national programmes was a major task to be taken up.

2 Organization

2.1 Overview

Cadlab is a joint venture of Paderborn University and Siemens Nixdorf Informationssysteme AG (SNI). Each partner provides scientific staff and corresponding financial resources to about equal parts. The cooperation is regulated by a contract closed between the two partners in agreement with the state of North-Rhine-Westphalia in 1985. It is open for new interested partners.

According to the guiding vision of deeply integrating university research and industrial development, a joint organization has been established, which enables Cadlab to act as one uniform organizational entity in a similar manner as an independent enterprise (see Figure 1). In formal external relations (e.g., in contracts with third parties), however, Cadlab does not act as a legal entity, but is formally represented by its two partners.

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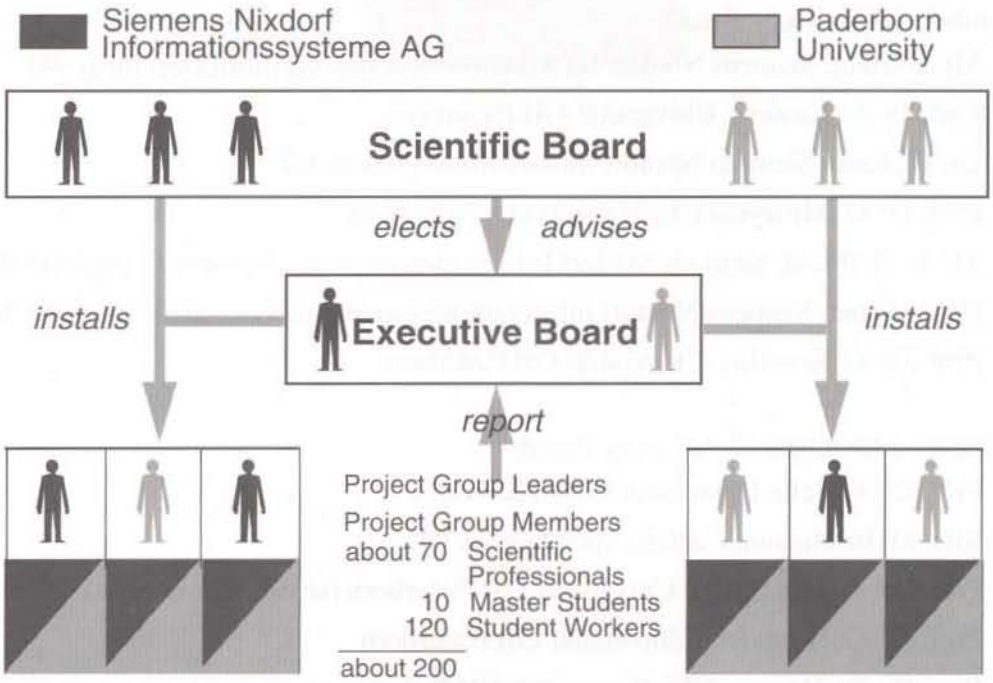

Figure 1 Cadlab, Principal Organisational Structure

Cadlab is headed by an executive board of two directors, one from the university and one from SNI. The executive board of directors is assisted and controlled by an advisory board, in which the interests of the partners are balanced.
All technical work is carried out in mixed project groups irrespective of the employment contract (industry or university) of the individuals. These mixed project groups are headed by project group leaders. Depending on the specific needs, these principal entities can be combined into larger "super project groups" or further sub-structured into smaller working groups. In particular, the project groups in the domains of "Information Technology" and "Electrical Engineering" have been combined into the corresponding super project groups "Information Technology, IT" and "Analog System Engineering, ASE" respectively.

2.2 Board Members

During the report period the following members were assigned to the Cadlab Executive and Advisory Board respectively.

Executive Board of Directors:

- Prof. Dr. F. J. Rammig, Universität-GH Paderborn
- Dr. B. Steinmüller, Siemens Nixdorf Informationssysteme AG

Chairman of the Advisory Board:

- Prof. Dr. W. Hauenschild, Universität-GH Paderborn

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Members of Advisory Board:

- Mr. G. Held, Siemens Nixdorf Informationssysteme AG (until December 94)
- Prof. Dr. U. Kastens, Universität-GH Paderborn
- Dr. W. Kern, Siemens Nixdorf Informationssysteme AG
- Prof. Dr. G. Mrozynski, Universität-GH Paderborn
- Mr. U. Rethfeld, Siemens Nixdorf Informationssysteme AG (since December 94)
- Dr. A. Sauer, Siemens Nixdorf Informationssysteme AG (vice chair Advisory Board)
- Prof. Dr. G. Szwillus, Universität-GH Paderborn

Associated Members of Advisory Board:

- Prof. Dr. F. Belli, Universität-GH Paderborn
- Mrs. M. Brielmann, Cadlab (since January 94)
- Prof. Dr. J. Gausemeier, Universität-GH Paderborn (since December 94)
- Prof. Dr. G. Hartmann, Universität-GH Paderborn
- Prof. Dr. W. Hauenschild, Universität-GH Paderborn (chair of Advisory Board)
- Mr. H. Heckl, Siemens Nixdorf Informationssysteme AG
- Mr. T. Kathöfer, Siemens Nixdorf Informationssysteme AG (until December 94)
- Prof. Dr. H. Kleine Büning, Universität-GH Paderborn
- Prof. Dr. T. Lengauer, GMD
- Prof. Dr. B. Monien, Universität-GH Paderborn
- Prof. Dr. F. J. Rammig, Universität-GH Paderborn
- Dr. B. Steinmüller, Siemens Nixdorf Informationssysteme AG
- Mr. H. Vogt, Siemens Nixdorf Informationssysteme AG
- Mr. J. Wening, Cadlab (until January 94)

3 Summary of Progress

Work in the report period was driven by the mission and goals summarized in chapter 1 above.

A key decision taken at the beginning of the report period was to form a new super project group called "Information Technology IT" (see Chapter 4) by merging two former closely related Cadlab main groups, and to subsequently form new subgroups in the areas of "Data Integration and -Modelling DIM", "Human-Computer Interaction HCI"and "Process- and System Modelling PSM". This way closely linked know-how areas could be united and strengthened, while at the same time the coarser organizational bundling created more degrees of flexibility for addressing new challenges on the project level.

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Key results that were provided by IT included advanced software prototypes and first product components in line with the given work programme. Moreover, a large number of research results - including five dissertations - have been published.

In the area of "Data Integration and -Modelling DIM" (see Chapters 4.2) considerable progress was made in the construction of an advanced software environment for product data modelling based on the international ISO-standards "STEP" and "EXPRESS". Here the front-end of the Cadlab STEP/EXPRESS-Workbench was successfully completed and made available to beta-users on an international scale. In the future this workbench will be able to easily connect to a wide range of heterogeneous, distributed databases as found in any large company. The mechanisms for this connection are currently developed under the name "Open Database Middleware (OpenDM)". OpenDM addresses the requirements of database federation, integration, migration and data independence and thus provides answers to urgent database management problems in industry and commerce. In the report period a first version of OpenDM was successfully tested in a pilot project in the SNI factories for midrange systems.

In the area of "Process and System Modelling PSM" (see chapter 4.3) the project on "Intelligent Framework Services IFS" was continued. IFS provides integrated object oriented software services for the processing of hybrid knowledge and the efficient construction of knowledge-based integrated applications. It extends the international IEEE/IMKA standard on frames with description means for rules and uncertainty parameters and provides a ready-to-use IFS-tool kit to the application programmer. In the report period the design work has been completed and first prototype applications have been developed. Thereby particular attention has been given to new application domains, such as traffic modelling and optimization, where interesting industrial projects have been conceived. Besides IFS, work on extended predicate transition nets (Pr/T-Net) was continued. Pr/T-Net concepts have been generalized and their application to support tool management was shown.

In the area of "Human Computer Interfaces HCI" (see Chapters 4.4), the project on "Advanced Editing Services AES" was carried on. A key achievement of this project was the provision of a comprehensive C++ library "Editor Operating System EOS" providing 350 classes and 4000 methods for the efficient construction of advanced platform independent editing systems. The EOS-libraries are already in use internally as well as externally. As an example, the graphical frontend EXPREME 1.0 of the STEP/EXPRESS Workbench (see above) and the EMC-Editor SCALOR 1.0 (see below) were built with EOS.

New challenges for IT and Cadlab are given by the upcomming "information society", which will also revolutionize the way complex information contents is exchanged by using the emerging super information highways. In the report period, Cadlab took part in the analysis and conception of new global electronic market places for complex information exchange. Cadlab helped to shape the new "GEN"-initiative on "Global Engineering Networks", whose mission is to initiate and coordinate new projects for the promotion of GEN-technology and GEN-marketplaces".

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The activities in the domain of "Analog System Engineering ASE" (see chapter 5) are focused on the development of tools and methods for the design of electronic circuits and systems under EMC-constraints. EMC stands for "Electromagnetic Compatibility" and addresses a problem area, which has become ever more critical with the adventure of high speed electronic systems. Effective solutions in this area necessitate the anticipation of EMC-effects early in the design process by means of sophisticated computer aided design and analysis techniques ("concurrent engineering"). Moreover, there is a strong need for EMC-consultancy throughout the field.

The central result achieved within ASE in the report period was the successful finalization of the EMC-Workbench V1.2 and its transfer into a newly founded spin-off company. Moreover, three dissertations and numerous publications shaped the scientific reputation of the group.

While much energy had been invested during the last report periods to industrialize the results and to investigate effective pathes for the commercialization of this advanced technology, in this report period the decisive break-through was achieved. After intensive negotiations with investors, the company INCASES Engineering GmbH was founded in Paderborn in November 1995. Key development and consultancy staff was transferred to INCASES together with EMC-technology, in particular the EMC-Worbench 1.2. At the same time work on forthcoming versions, which will pay particular attention to systems aspects, continued. A close cooperation has been set-up with INCASES in order to safeguard the smooth technology transfer of new solutions.

Consultancy of SNI and Siemens factories also played a significant role during the report period. For example, the most critical parts of new SNI UNIX computers (RM Family) were successfully prepared and analysed for electromagnetic compatibility and signal integrity. The consultancy services have also been successfully transferred to INCASES at the end of the report period.

Besides the technology transfer task, the re-orientation of the ASE-group towards future topics was continued. Here, the development and application of EMC-technology to full systems on the micro- as well as the macro-level is of primary interest. In the report period most of the work focused on the micro-level. Moreover, a new organizational set-up has been prepared.

Efficient support for the ongoing R&D work was provided by the Cadlab "Technical Management Group" and the "Computing Centre, CC" (cf. chapter 6). CACE-consultance provided to the SNI System Unit Midrange during this and the last report periods not only supported the application-oriented approach of our technical main groups, but also laid the basis for new joint consultancy projects, which will become effective in the next report period (project data management, application of data base middleware know how, a. o.). Moreover, internal quality assurance and computing support was provided.

During the report period most of the technical tasks and staff migrated into the technical groups. As a result a lean "project support group" has been founded, which is responsible for administrative and marketing support tasks.

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While some of the central tasks have been transferred into the main groups by the end of the report period, "parallel computing" was taken up as a new technical topic for the CC-group. Initial studies have been undertaken in preparation of new project fields.

Most of Cadlab's work again was carried out in the context of collaborative projects (see chapter 8). Concerning nationally funded collaborations, Cadlab has participated in 7 BMBF projects, two of them executed in the frame of the European JESSI programme. Thereby, the large European EMC project JESSI AC-5 is also led by Cadlab. Three projects are funded by ESPRIT.

Publications and dissemination of technical/scientific results again played a major role also in this report period (see chapter 7). Cadlab's work is documented in about 120 public reports and papers. Cadlab software was demonstrated on more than 10 fairs all over the world including in Japan, USA, Canada and many EU-countries. More than 80 formal presentations, talks and tutorials were given on a large number of international events. At the same time internal technology transfer, education and training of young talent in application oriented engineering was actively promoted. This is reflected by 10 master theses written under the supervision of Cadlab members and 120 student assistants integrated in a large number of Cadlab software projects.

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II Project Group Reports

4 Information Technology - IT

4.1 Introduction

The project group "Information Technology, IT" was formed in April 1994 as a merger of the two former project groups "Base Technology, BT" and "System Engineering Technology, SET". The rationale behind this merger was the fact that in both groups large potential for synergy and cooperation has been identified, which made it necessary and sensible to join forces.

In continuation of the existing activities started in BT and SET in 1993 three project groups have been founded with the following objectives:

- the Data Integration and Modelling group, DIM, combining the work of the former BT group Data Integration (DI) on data base federation services, DBF, with the STEP/EXPRESS data modelling efforts of SET; starting point of the work of DIM has been the joint objective of offering open data base middleware services for the efficient, transparent storage of, access to and interchange of data in heterogeneous data base environments; the heterogeneity relates both to data base technologies in use (file system based, hierarchical, relational and object-oriented ones) and the platforms (PC and UNIX systems) on which these data bases are operated.

- the group Process and System Modelling, PSM, which emerged from the two groups Control Integration (BT CI) and System Engineering Technology (SET); both groups were dealing with two different views on heterogeneous IT systems: An operational view modelled by Extended, Timed Predicate/Transition-Nets (Pr/T-Nets) and a declarative view expressed by rules and frames; in combining these approaches, PSM performs research and development in the area of computer-based system specification, evaluation, generation, and control; the target is the development of integrated, generic environments for system development and system control;

- and the Human-Computer Interaction group, HCI, as natural successor of the BT group User Interface (UI) to give credit for its broader topics like gesture-based editing and visual programming, both in development and research; in parallel, all Cadlab efforts on editors and graphical representation means as generally available services for all the other Cadlab project groups have been bundled in this group;

All the efforts spent and work done by IT during the report period were originating from BT's former mission to investigate infrastructures needed for the engineering of computer-based systems and to provide basic services for building engineering environments and from SET's mission to perform research and development in the field of concurrent system engineering methods and tools.

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4.2 Data Integration and Modelling - DIM

4.2.1 Baseline

The access to and modelling of data gains increasing importance since database applications are not even more restricted to single data sources. An increasing number of database applications is confronted with problems in the area of

- data access to and manipulation of multiple heterogeneous databases
- integration and modelling of data crossing multiple data bases
- exchange of data between application domains and user sites
- migration of data and migration of applications

In most of these cases either multiple database applications or multiple databases are involved. A scenario were multiple applications run on multiple databases makes this expressive. We use this scenario as a guidance for our R&D work. The idea is to provide a software layer as a kind of database middleware between applications and data handling systems (database systems, file systems, etc.) which allows to reduce the efforts and costs for designing and implementing database applications.

4.2.2 Work during the Report Period

4.2.2.1 Database Federation Services

The "Database Federation Services (DBF)" project started in January 1993. The aim of the project is the federation of heterogeneous, autonomous database systems (DBS).

Object-oriented database systems together with database systems based on the most relevant relational or the entity-relationship model are candidates for the federation within the DBF project. Efendi - one result of the DBF project - offers a solution in form of a flexible software layer on top of these heterogeneous database systems. It allows to preserve the autonomy of these "component databases (CDB)" so that their existing applications can continue to run locally (keyword: preservation of investment). On the other hand, it offers uniform and transparent access to the "federated data" of the CDB for new (global) applications. The architecture of Efendi can be seen in Figure 2.

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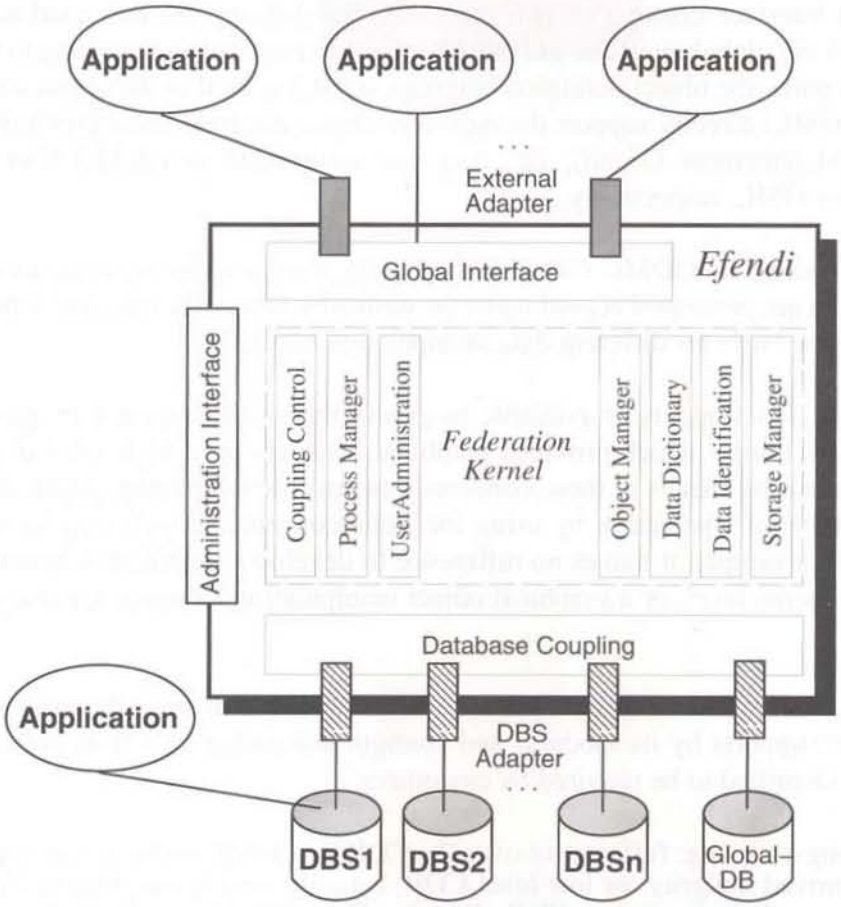

Figure 2: Architecture of Efendi

The model contains the following modules:

- Administration Interface: supports administration facilities
- global interface: providing multiple federated and external schemata and furthermore operations according to them;
- external adapters: data model conversion between standard database interface, e.g., STEP/SDAI used by a global user and Efendi Global Interface; an External Adapter is only needed if the Global Interface and the user required database interface differ;
- federation kernel: connecting link between user resp. application and CDB, deals with necessary mappings and transformations;
- database coupling adapters: data transport and conversion between heterogeneous, federated data base systems and Efendi (with a canonical data model);
- CPU DB: storing global data, meta data and schema information of Efendi.

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The global interface consists of two parts: one for defining the federated and external schemata of the global interface and one for object manipulation according to these schemata. Both parts, the object definition language (ODL) as well as the object manipulation language (OML) directly support the industrial object database standard ODMG (Object Database Management Group), i.e., they are compatible to ODMG C++ ODL and ODMG C++ OML, respectively.

Instead of coding the ODMG C++ OML by hand, interfaces for schema consistent data manipulation are generated according to the defined schema. By this, one schema definition can be the basis for different data manipulation interfaces.

Furthermore, functionality is available to extend the global interface by graphical features. A C++ library which provides graphical concepts on a high level of abstraction was developed. By means of these concepts it is possible to develop graphical editors on different levels of abstraction by using the same concepts. Concerning these graphical concepts, for example, it makes no difference to develop a graphical schema editor representing schema level, or a graphical object manipulation language representing object level.

The application of Efendi is not restricted to the federation of some database systems but Efendi also supports by its modular and configurable nature two other solutions which have been identified to be required by customers:

- strong-coupling: full control over the CDB by Efendi, no local users/applications, improved integrity for low level CDB, e.g., file system (see Figure 2); by way of "Strong-Coupling" one CDB, Efendi offers data base independence (database middleware) by hiding DB-specifics form the application programmer;
- migration: tool and data migration (see Figure 3).

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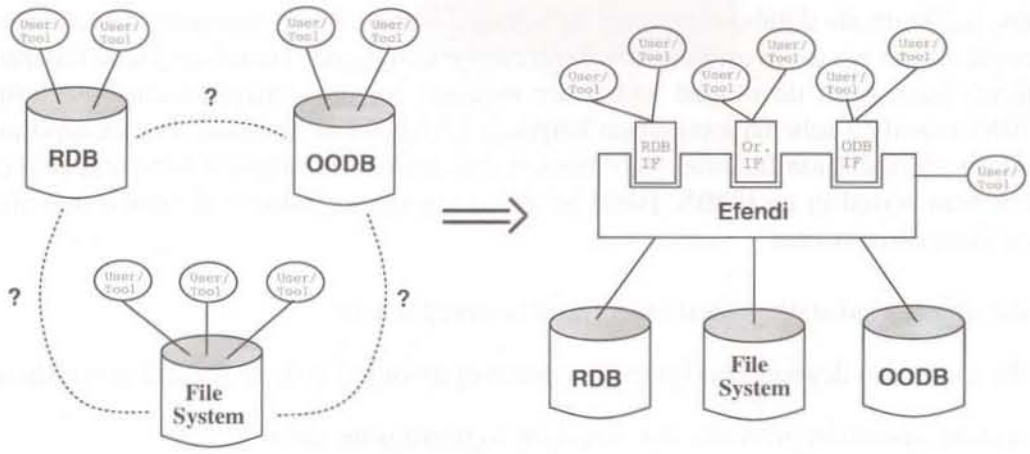

– no local users
– no autonomy of CDB (more concurrency control)

Figure 3: Strong-Coupling of CDB

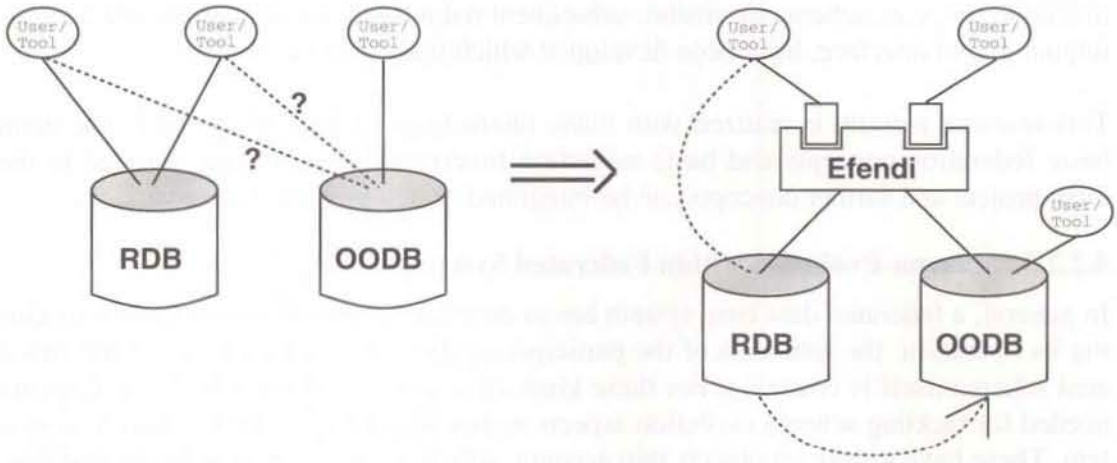

Figure 4: Tool and Data Migration

The DBF project follows the SNI Process Technology and is now in the "Implementation Phase". In parallel to this phase, the development of a graphical Efendi demonstrator and a pilot project with a SNI department has been started. The demonstrator couples the relational database ADABAS-D and the object-oriented database SIFRAME-OMS.

In the pilot project also a relational database DDB/4 has been coupled with a file system based electronic library and a relational PC database ACCESS.

4.2.2.2 Federation of and Migration Within Multiple Database Systems

While existing approaches treat the federation and migration among multiple heteroge-

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neous, autonomous database systems as separate issues, these, currently more research oriented efforts are to investigate how both can be combined. Therefore, basic federation concepts have been developed which are required for any federated database system (FDBS), mainly a schema integration language and a global interface. For incorporating novel object migration facilities into them, it was at first investigated what and how data can be transferred in an FDBS. Baseline was a migration framework which is scalable along three dimensions:

1. the object kind stating what object data is stored where,
2. the migration degree specifying how much of an object to transfer and from where,
3. and the operation primitive defining how to transfer the data.

At Cadlab, implicit and explicit migration operations which enable users/administrators to transfer data among the various database systems in various granularities have been developed during the report period. All migration operations preserve the objects global identity. Thereby data locality change is hidden from global FDBS applications so that they do not have to be recoded. While the basic federation concepts in combination with the object migration functionality allow to cover many migration cases, extended federation concepts, e.g., schema extension, subsequent redundancy identification, and a multilingual global interface, have been developed which make it even broader.

This research activity is realized with many interactions to the DBF project. The main basic federation concepts and basic migration functionality are already adopted in the DBF project and further concepts can be integrated seamlessly into future versions.

4.2.2.3 Schema-Evolution within Federated Systems

In general, a federated data base system has to deal with a number of modifications during its operation: the schemata of the participating data bases may change or the federated schema itself is changing. For these kinds of schema evolutions basic methods are needed for tackling schema evolution aspects within the overall federated data base system. These have to take all objects into account, which are affected by schema modifications. In parallel to the necessary research in this area prototype-like software components are being developed for sample practical judging of the chosen approaches in order to get early feedback.

4.2.2.4 STEP/EXPRESS Environment

The project STEP/EXPRESS Environment was started in the beginning of 1993.

The emerging international standard for the exchange of product model data is ISO 10303 "Industrial automation systems and integration -- Product data representation and exchange", better known as STEP (STandard for Exchange of Product data). STEP provides standardized data schemas, called *Application Protocols (APs)*, for a number of application domains. For defining the data schemas, STEP provides the information modelling language EXPRESS. Thus, the APs are annotated EXPRESS schemas.

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The STEP implementation methods define the implementation of data exchange and data access. The implementation methods are independent from any specific EXPRESS model. Part 21 of STEP defines how an ASCII file format is derived from an EXPRESS schema.
Thus, an AP together with Part 21 defines a standardized file format for data exchange. Part 22 of STEP defines the database interface SDAI (Standard Data Access Interface), which provides a standardized access to data that conform to an AP.

Figure 5 shows the Cadlab view of a STEP implementation. The data are stored in a database or a number of (heterogeneous) databases. The application(s) access the data via the Standard Data Access Interface SDAI. For the data exchange, a writer and reader are provided that write the data to be exchanged in a STEP File or read it from a STEP File.

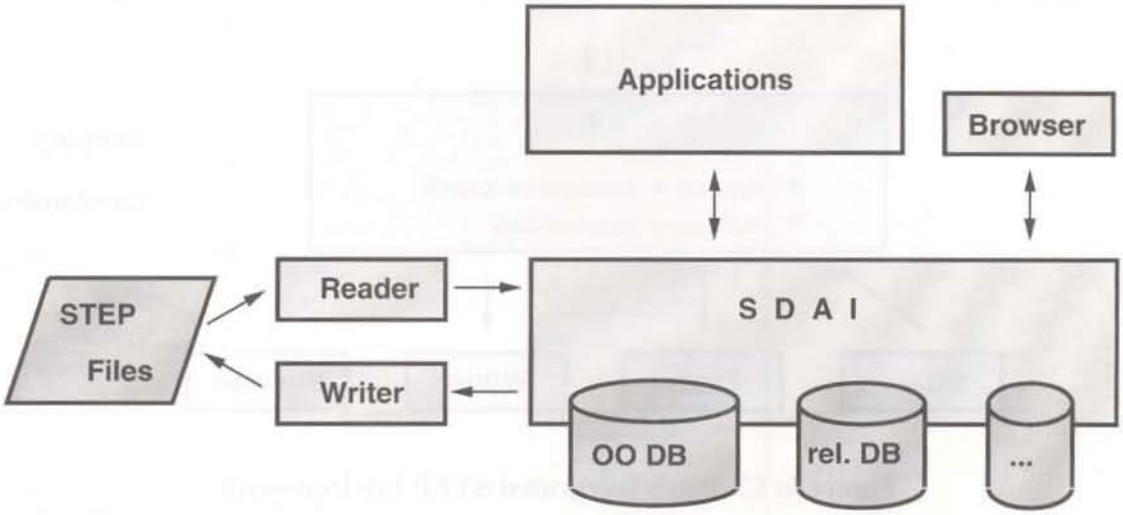

Figure 5: Product Data Access and Exchange

The basic idea of this work is the generator approach. Since an EXPRESS model automatically defines the file format for data exchange and the SDAI, the corresponding STEP software can be generated automatically from EXPRESS models. Therefore, Cadlab does not implement the SDAI or reader/writer themselves, but implements generators that generate this software from the application data schema (EXPRESS model). Figure 6 gives an overview of the integrated Cadlab STEP environment.

For the design of EXPRESS models, the EXPRESS-G editor EXPREME was developed in cooperation with the HCI group, see Chapter 4.3.2.2. In 1994, the delivery of EXPREME 1.0 was started. Now EXPREME 1.2 is marketed by SNI. Over 70 licenses are installed world-wide.

In 1993, the EXPRESS syntax and semantics checker ICE was developed. Since November '93, ICE is available free of charge for Sun-4, SGI, HP9000, Apollo, IBM RS6000, OS/2, and Linux. The ICE software can be retrieved from the ftp server of Paderborn

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University via anonymous ftp. During the report period, ICE was adapted to the ISO 10303-11 International Standard, and ICE was prepared to serve as front-end for the generators.

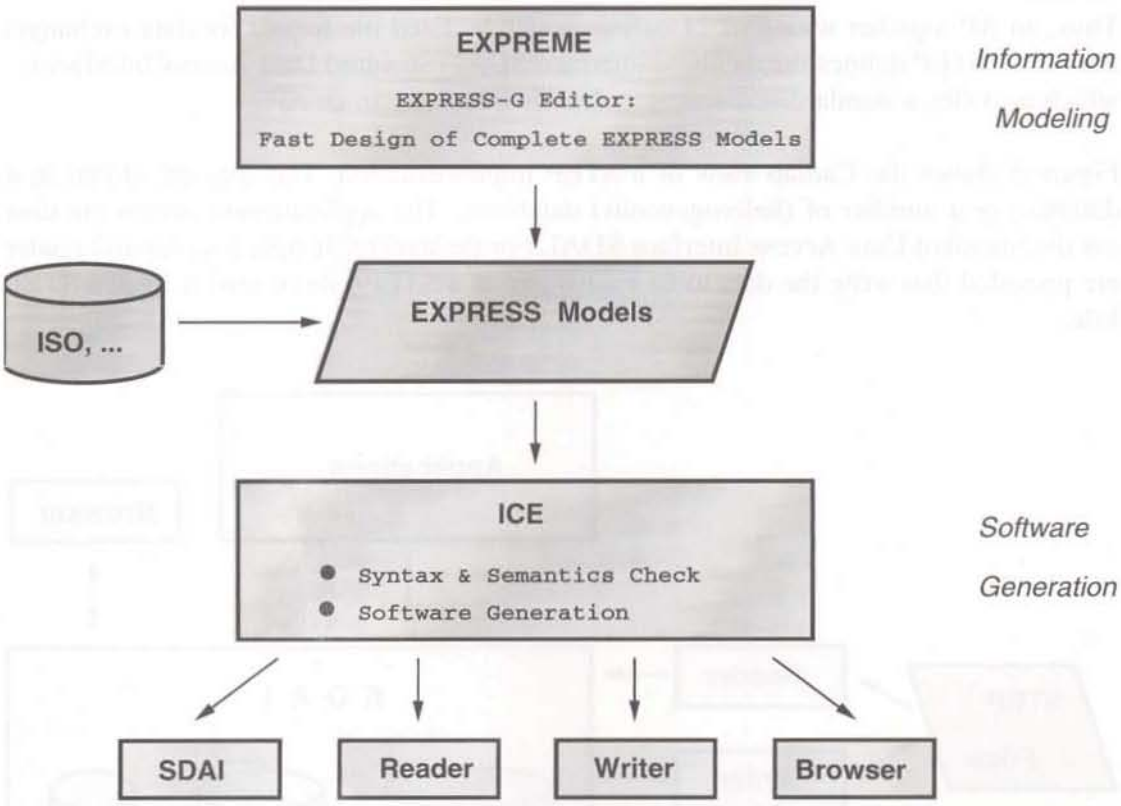

Figure 6: Cadlab's Integrated STEP Environment

The first generator built was an EXPRESS-to-TIDL generator. TIDL is the Data Definition Language of SIFRAME/OMS. The EXPRESS-to-TIDL generator was completed during the report period and was delivered to a number of users within SNI.

Furthermore the development of the SDAI generator was started during the report period. SDAI is the Standard Data Access Interface of STEP. A generator is being developed that generates a C++ early-binding SDAI implementation from a set of EXPRESS schemas. This generator is based on the software realised within the DBF project: A generator was developed that generates the ODMG C++ OML from an ODL data schema, the SDAI generator generates the SDAI from an EXPRESS data schema in a similar way.

4.2.2.5 Transaction Management in Design Environments

An important aspect of design environments is design transaction management. Design transactions are different from traditional transactions as they have to support long-lived and cooperative activities. Known algorithms for concurrency control and recovery are too restrictive for such environments. Thus, a lot of advanced transaction models have been developed throughout the last few years that try to support design and other cooper-

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ative applications. However, a satisfactory model offering the flexibility needed by design environments is still an open research issue. In particular, there are only few approaches to the problem of recovery of design transactions.

Cadlab has therefore developed a transaction model for the area of design which is based on the transaction toolkit approach (developed at the University of Hagen). The model offers flexible concurrency control and recovery strategies which can be configured in an application-specific way. The model also aims at the integration with an object-oriented database system (following the ODMG Standard) in order to exploit semantic information from the database schema. In order to demonstrate the practical applicability of the concept, Cadlab has developed a prototype of the transaction model.

4.2.2.6 An Open Object-Oriented Integration Environment

Integration of tools into a design environment means to add tools into this environment and let them interact with other tools within the environment. This includes the organisation of data so that they can be shared by different tools as well as a common control mechanism for the coordination of control flow of tools. Whereas the organisation of data mostly is a structural aspect, the coordination of tools mainly is a behavioural aspect. Both aspects must be combined into a common abstract data model. The object-oriented approach supports both aspects in a proper way but it lacks a standardised object-oriented data model so far.

These requirements motivated the investigation of an integration model containing object-oriented basic concepts which can be applied recursively to be configured to domain specific data models and data schemas. These concepts are on one hand still object-based and allow on the other hand the definition of particular concepts. As a result of the recursive approach the structural and behavioural coordination of different data models and data schemas as well as the definition of different application domains is handled in a unique manner. Based on these basic concepts different levels of tool integration, the integration of domain specific and domain neutral tools, as well as the specification of tool-specific interfaces to data shared by several tools are supported.

4.2.2.7 A Rule Meta Model for Active Database Systems

Rules are used in active database systems to monitor situations of interest and to trigger a timely response when these situations occur. They can be applied for several problems, e.g., consistency checks, derived data, change notification or recovery. The integration of rules into database systems does not only have advantages - the main drawback is the introduced complexity which makes it more difficult to understand what happens in the system and which is the source of additional inconsistencies as, e.g., infinite loops, where rules trigger one another indefinitely. A rule model defines the semantics of the rules and how a collection of rules is treated at run-time. Rule meta models offer a set of parameters which can be used to define rule models.

Rule meta models are useful for a couple of reasons, e.g., they offer a good baseline to compare existing rule models, they can be used as baseline for the analysis whether rules may trigger one another infinitely and they can be used to define rule semantics which

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best fit to the requirements of the applications. Existing rule meta models only offer parameters for parts of the semantics of rule models, and some of these parameters do not describe elementary rule model aspects. Therefore, a rule meta model has been developed which should fill this gap. This model uses Petri Nets as a formal method for a precise specification of many of the different aspects of rule modes.

4.2.2.8 Semantics and Definition of Structural Defined Views

The majority of view models for object-oriented database systems (ooDBS) has extended the semantics of relational views by utilizing and applying the new opportunities of ooDBS, e.g., object identity. New features of view models also support the use of views for advanced applications that go far beyond the traditional relational views. In particular, views are conceived as application specific schemas on top of the conceptual database schema. But so far, no widely accepted notion of views in ooDBS exists.

In spite of the non-uniform semantics of views in ooDBS - a lot of new indispensable new features, new requirements, and new technical solutions - the majority of view models are based on the traditional mechanism for view definition: Views are defined by means of a query, i.e., the result of a query is conceived to be the view. But an object-oriented data model provides two mechanisms for view definition: an operational one, based on a query language, and a structural one, based on inheritance mechanisms. So far, the latter one hasn't received much attention in literature.

Current research activities at Cadlab concerning views in ooDBS focus on the structural definition of views. The following aspects are examined:

- What do operational and structural view definitions have in common and where do they differ?
- What are strength and weakness of operational and structural view definitions?

The research results show that operational view definitions lead to problems concerning pretentious data representation within the view while structural view definition in its pure kind isn't suitable to define views that satisfy predicates on object values. To overcome the weaknesses of the structural as well as the operational view definition it is recommended to integrate both kinds of view definition in one common framework resp. architecture. The research activities lead to a view model for structural view definition that satisfies pretentious data representations, e.g. restructuring of objects and attributes. According to the proposed architecture, the view model can be integrated with operational mechanisms for view definition.

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4.3 Process and System Modelling - PSM

4.3.1 Baseline

Since information technology plays a key role in linking several technologies like mechanics, communication, transport, or business systems, engineering environments have to consider these heterogeneous application domains. In order to tackle this variety of technical and organizational systems an integrated core environment is being developed. This core environment provides application independent models, methods and tools that can be easily specialized for the envisaged application domains, e.g. in order to provide a user with the specification formalisms he or she is used to. The core environment will be applied in the development of mechatronic, hardware engineering and transportation systems. The methods and tools of the core environment are not only useful for heterogeneous system development but also proved their applicability for the control and guidance of system development processes.

Depending on the point of view towards the systems under design, different requirements arise with regard to the specification and interpretation of system models. If primarily the system behaviour is regarded an operational model is preferable. If the concrete system behaviour (e.g., sequencing, parallelization or timing of actions) should be abstracted a declarative view seems to be more appropriate. Accordingly the core environment provides two formalisms for system specification, evaluation and generation. Extended timed Predicate/Transition-Nets (Pr/T-Nets) are used to describe behavioural aspects of systems or system parts. Rules and frames are provided as declarative modelling formalism. One major advantage of these modelling formalisms is that the semantics of system descriptions is clear and unambiguous since also the interpretation of these models is formally defined.

However, these modelling formalisms do not allow to tackle raw information like pictures, which will become more important with the extended use of multimedia environments. Therefore, the core environment will be extended by mechanisms to analyse pictures of systems or system parts and to combine this information with the corresponding symbolic description.

4.3.2 Work during the Report Period

During the report period work was carried out on software platforms for the declarative and the operational branch of the core environment, that are described in respective paragraphs on "Intelligent Framework Services" (see chapter 4.3.2.1) and "Pr/T-Net Modelling and Simulation Environment" (see chapter 4.3.2.2). Some applications of the underlying modelling paradigms for system specification and evaluation will be described in the paragraph on "System Modelling and Evaluation" (see chapter 4.3.2.3). Design activities concentrated on the observation, development and realization of "Hardware Design Methodologies" (see chapter 4.3.2.4). As a cross-cut activity through different application domains and engineering activities work was performed on "System Design under Timing Constraints" (see chapter 4.3.2.5). Further work was performed on the "Evaluation of the JESSI-Common-Framework".

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4.3.2.1 Intelligent Framework Services (IFS)

The "Intelligent Framework Services (IFS)" project started in January 1993. The aim of the project is to provide hybrid knowledge representation and evaluation services and to help system developers in building knowledge based tools. For the IFS project no new knowledge processing approach has been looked for, but instead the system is built on top of the concepts which have already proven as an expressive means of dealing with knowledge, namely on *frames* and *rules*. However, different to all other known hybrid knowledge-representation system known, the frames and rules components of IFS are deeply integrated using the object-oriented paradigm, and their integration incorporates possible extensions to handle uncertain knowledge. To ensure that end user needs are considered, a set of application examples have been built using IFS.

The work for IFS was largely carried-out in the JESSI Common Frame (JCF) project. Within the subproject 'Applied Research' (SP1) prototype software was provided which consists of a knowledge representation and access component (KAL) and a knowledge evaluation component (KEC). Within the subproject 'Development' (SP2) a transfer plan for IFS software components was defined which follows the SNI Process Handbook, PHB. According to these guidelines the prototype software developed within SP1 was improved and additional documentation required by the PHB was provided.

The problem independence of the IFS basic services allows for the development of various kinds of knowledge based systems differing in knowledge structure, problem solving strategy, and last but not at least the target domain. Nevertheless, all conceivable applications share the same basic components and properties. Figure 7 gives an overview of the main IFS software components, figures 8 and 9 give further details on the development and runtime views respectively

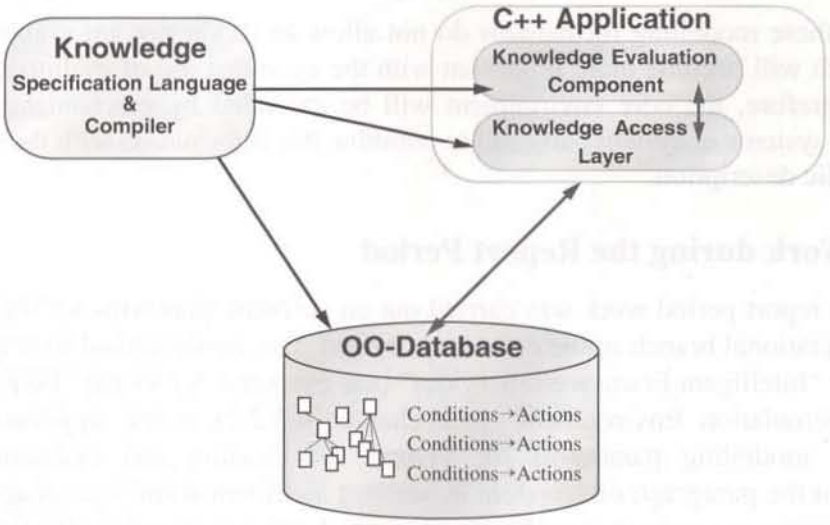

Figure 7: The IFS Software Components

To specify the knowledge base of an application and the desired inference control, a specification formalism is needed. In the IFS system, the knowledge specification lan-

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guage, HyKL (**Hy**brid **K**nowledge Description **L**anguage), is used to this end. A HyKL specification forms the knowledge schema of an application. A HyKL compiler translates this description into a persistent knowledge base residing in an object-oriented database. The IFS system is currently based on the JCF Development System, mainly on its object management system, OMS and on the object definition language TIDL. Therefore, the HyKL compiler is a cross compiler which generates TIDL code.

For the development of the frame-part of HyKL, a proposed IEEE standard is used as a base. This standard for a frame-based knowledge representation is developed by the IEEE working group P1252. Frames are the fundamental representational structure of choice for a wide variety of representational tasks. Each frame represents a concept and consists of a collection of attributes and their values, that are associated with that concept. Rules allow users to describe heuristics and procedural knowledge of a domain. If rules and frames are integrated, attribute values can be tested within rules. Rule premises inherently define semantic proximity between attributes of different objects. Thus, when integrated with frames, rules give a very general way for defining arbitrary semantic relations in a frame-based representation system.

To access a knowledge base specified by HyKL, an interface in form of the Knowledge Access Layer (KAL) is provided. KAL combines different knowledge representation paradigms to achieve both high expressiveness and reasonable performance, enabling the development and integration of employable knowledge based systems consisting of a persistent knowledge base.

The Knowledge Evaluation Component of IFS (KEC) provides an inference engine to efficiently evaluate knowledge structures, but applications may also implement their own problem solving strategies and user interface for knowledge acquisition and case description using the IFS Knowledge Access Layer (KAL). The Knowledge Evaluation Component of IFS supports forward chaining of production rules. Since HyKL integrates the paradigms of frames, production rules, and uncertain knowledge with object oriented database technology, the existing solution algorithms for forward chaining are extended especially with respect to means of database integrity and concurrency in multi user scenarios.

Some of the components mentioned are represented in Figure 8. Additionally, Figure 8 shows how an application is generated:

An IFS application developer writes a HyKL script from the conceptual model of the system to be built. He or she models the domain structure with HyKL frame structures and heuristics of the domain with HyKL rules. Procedural behavior of frames may be specified in method slots by triggering sets of rules or by writing functions or member functions in C++. For many problems and algorithms, the latter is more convenient than rules.

The knowledge base is completely accessible from C++ by function calls to the HyKL API. Method slots and slot demons defined by a C++ function must be adequately declared in the HyKL script. In Figure 8, this is illustrated by a thin arrow labelled 'refer-

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ences' in the legend. As further shown in Figure 8, the HyKL compiler generates a TIDL script. This TIDL script will be provided with all necessary information to identify a function according to a particular method or demon at runtime. Additionally, it contains the database representation of HyKL rules. Further, the HyKL compiler generates a so called external function manager, which dispatches all calls to methods and demon triggers to execute the appropriate function with the correct parameters during runtime. For HyKL Rules, the compiler also generates an internal, C++ coded structure for efficient matching of rule conditions. This structure and the external function manager have to be compiled and linked together with the function definitions coded in C or C++, the HyKL API library, and the library providing the runtime functionality of the Knowledge Evaluation Component KEC.

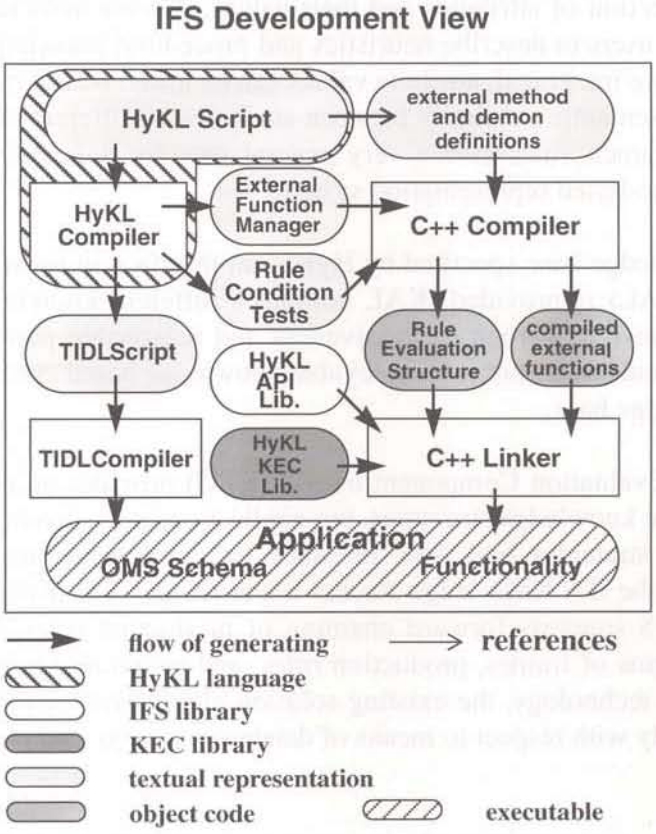

Figure 8: The IFS Development View

The rough module structure of the resulting IFS application is shown in Figure 9. The software consists of the pure application part, designed by the application developer. It has to be noted, that it may contain arbitrary C++ programming and OMS accesses besides frame and rule accesses, if needed. Access to the entire frame structure including schema information, instances and relations as well as to sets of rules, single rules and parts of rules is ensured by the HyKL API. The HyKL KEC provides for efficient rule evaluation by forward chaining. The KEC and the API should be divided in a database independent and a database dependent part, for reasons of portability. The External Function Manager which dispatches demon calls triggered by database accesses or method calls is generated by the HyKL compiler.

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The approach pursued by the IFS project has been justified by applying the developed IFS technology in two areas: An advisory system for EMC evaluation purposes and traffic optimization employing intelligent services have been successfully demonstrated.

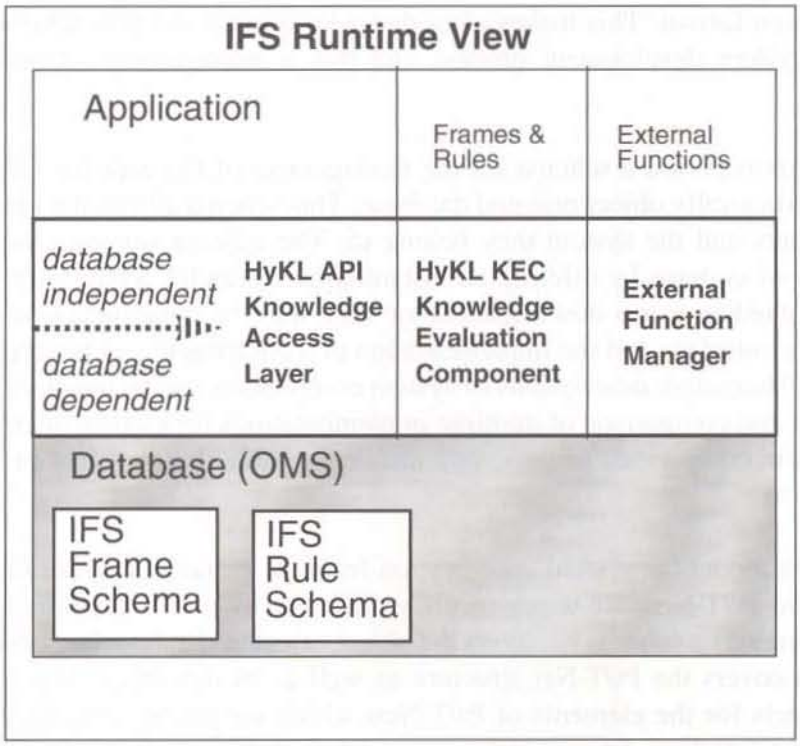

Figure 9: Functional Architecture of an IFS Application

4.3.2.2 Pr/T-Net Modelling and Simulation Environment

During the report period a prototype of a design environment for extended Pr/T-Nets was developed. With this environment it is possible to specify and simulate extended Pr/T-Nets. The main features of extended Pr/T-Nets are:

- set operations at transitions,
- hierarchical places and transitions,
- time dependent firing of transitions,
- recursive definition of hierarchical nets.

The Pr/T-Net environment is based on a common data schema that covers the management of design data in general and a data schema for the net representation itself. These schemata will be described first before an overview of the Pr/T-Net environment is given.

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Schema Development:

Complex systems consist of a lot of different components from different application areas which might be handled by different tools of the system engineering environment. These tools might work on a common data format. But very often they also need their own description format. This makes clear that a lot of data and files have to be handled during the system development process and that a management schema is urgently needed.

Within the report period a schema for the management of the data has been developed based on a structurally object oriented database. This schema allows the identification of the components and the system they belong to. The schema supports the hierarchical development of systems by offering an instantiation hierarchy. Systems or system parts may be designed in a top down manner or they may be constructed in a bottom up approach. The interface and the implementation of a component can be stored separately and different alternative descriptions of system components can be handled. This enables the definition and comparison of multiple implementations for a given interface. Already existing system components or those that reached a stable design status can be archived in libraries.

As a common model for system specification from the behavioural/operational point of view extended Pr/T-Nets are used. To allow different tools to work simultaneously on these specifications a schema based on the object oriented database has been developed. This schema covers the Pr/T-Net structure as well as its dynamics. The structural part contains objects for the elements of Pr/T-Nets which are places, transitions, edges and the ports of the interface. Special instantiation relations are introduced to allow access to the instantiation facilities of the data management schema and thus to the instantiated subnets. The schema part for handling net dynamics allows to manage graphs of net states. Each net state consists of objects representing the actual marking and the transition status.

For both schemata, the management schema and the net schema, C++ classes for the schema objects and access methods as programming interfaces have been developed and implemented. Based on these programming interfaces the Pr/T-Net Environment described in the next paragraph was realized.

Overview of the Pr/T-Net Environment:

The current environment consists of a browser for the selection of existing or new nets or subnets, a Pr/T-Net-Editor for a comfortable editing and simulation of Pr/T-Nets, and a Pr/T-Net-Interface-Editor for the definition of abstract graphical representations for subnets. Some important features of the design environment are:

Mixed Editing and Simulation of Extended Pr/T-Nets:
With the Pr/T-Net-Editor it is possible to edit and simulate the net alternately without intermediate compilation steps. During such an edit-simulate-sequence it is even possi-

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ble to change the actual net marking and continue simulation on this new marking. Markings reached during the simulation can be saved and reused as starting points for further simulation steps together with new markings generated with the editor. This feature allows a very flexible handling of stimuli which is especially valuable during the development phase of a system.

Mixed Top-down and Bottom-up Specification of Hierarchical Pr/T-Nets:
In the same design some parts may be specified in a top-down manner while other parts are specified in a bottom-up fashion. After completion of the specification the consistency can be checked explicitly. If the same subnet is used several times in a specification, only the dynamic net information is copied and the static information is instantiated. This avoids redundant storage of the same information.

Abstract Representations of Subnets:
With the Pr/T-Net-Interface-Editor an abstract representation for a subnet can be specified. If the subnet is used in the definition of another net, only this abstract representation is visible. During the simulation of the subnet the firing of a transition may cause a change of the abstract representation. Hence, the abstract representation reflects the state of the subnet. Figure 10 and 11 shows the Pr/T-Net-Editor during the simulation of a Pr/T-Net specifying the control of traffic lights at an intersection. In the net for the intersection the abstract representations of the subnet for the traffic light (instantiated twice) and the subnet for the control of the intersection are depicted. Below, the net definitions for these subnets with their actual states are represented. For example, in the subnet for the left traffic light the transition "Rot/Gelb" which means "Red/Yellow" has finished its firing cycle (its output place is marked). The abstract representation in the net for the intersection reflects this state.

4.3.2.3 System Modelling and Evaluation

As an application driven first step towards the integration of the declarative and operational branches of the core environment concepts for the evaluation and optimization of transport systems were developed. Based on a Pr/T-Net model of the transportation system its current characteristics can be evaluated using the Pr/T-Net simulator. Afterwards a rule based analysis and optimization of the simulation results will take place using the Intelligent Framework Services. As further application domains for the Pr/T-Net model mechatronic systems, the formalization of distributed backplane-based simulation, and the design assistance for an integrated hardware/software co-design environment were regarded.

Mechatronic Systems:

One special group of system regarded were mechatronic systems consisting of digital components, physical components and control components. For these systems a common modelling technique based on extended Pr/T-Nets was further elaborated. In addition to the difference equation approach developed during the previous report period the state based representation of analogue components is supported. A major advantage of the state based approach is that it eases the coupling of different analogue components. Fur-

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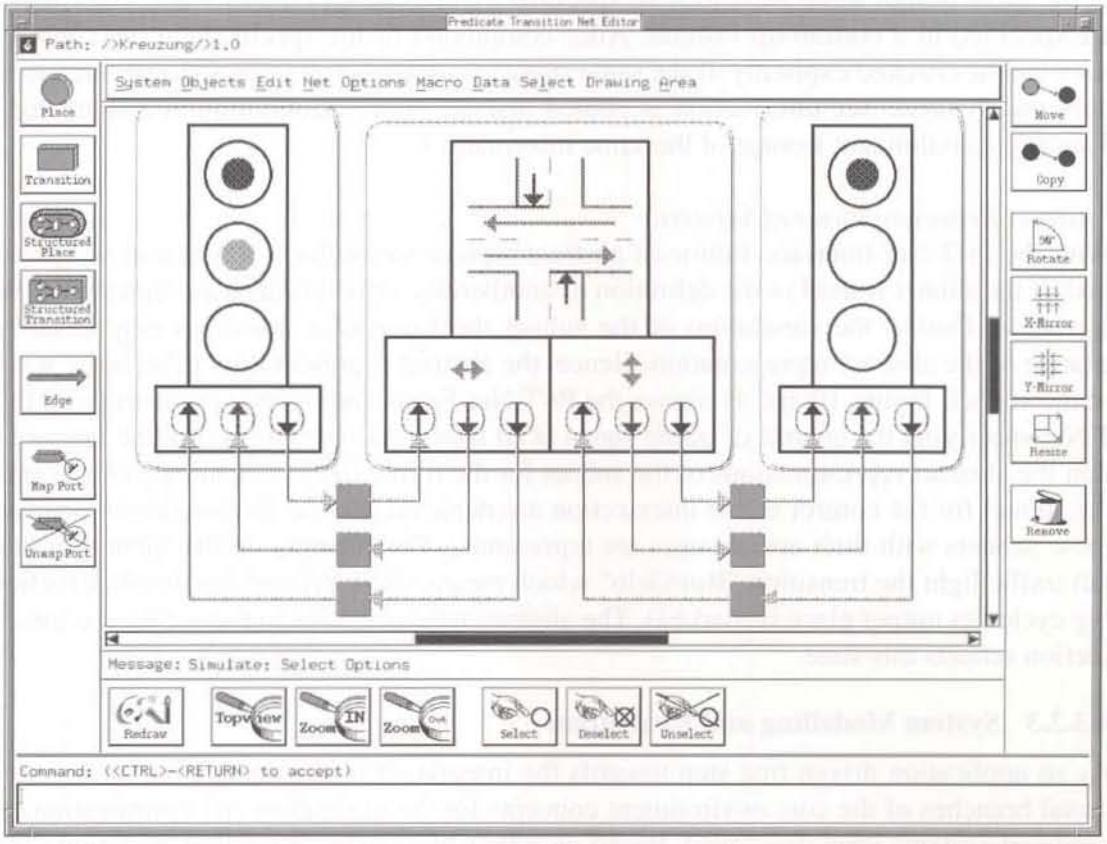
thermore, it is more commonly used for the description of physical and control components in mechatronic systems than difference equations. Within the report period a methodology has been developed which allows the modelling of state space representations by extended Pr/T-Nets. This methodology also provides solutions for the handling of nonlinear analogue components and for the coupling of different analogue components.



Simulate dialogue:

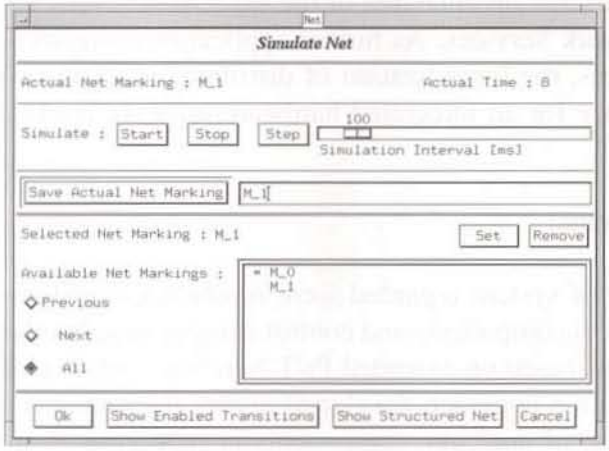


Figure 10: Simulation of Extended Pr/T-Nets (I)

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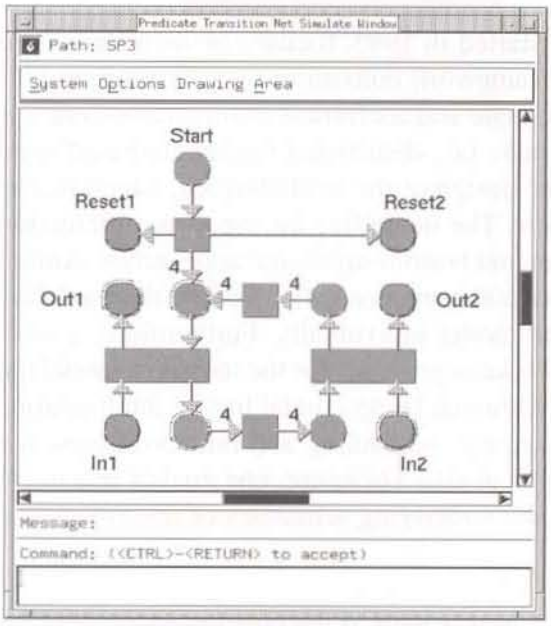
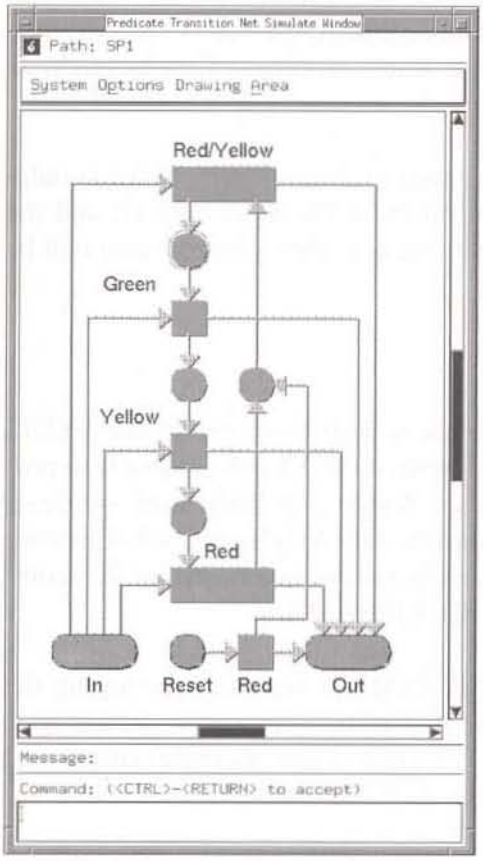
Net for intersection control:



Net for left traffic light:



Net for right traffic light:

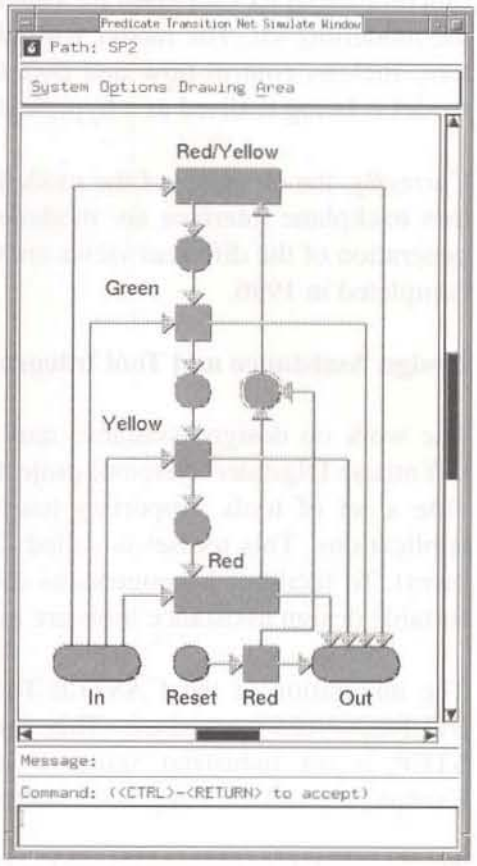


Figure 11: Simulation of Extended Pr/T-Nets (II)

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The Formalization of Distributed Backplane-based Simulation:

This research activity, started in 1993, focuses on the extension of the Pr/T-Net formalism into a modelling framework consisting of a "modelling kit" and the methodology how to use it. Both, rationale and usefulness of this framework are to be demonstrated by a complex modelling task, i.e., distributed backplane-based simulation. Therefore, one focus of this work is the design of the modelling kit, which is a set of well-defined high-level Pr/T-Net constructs. The modelling kit supports a hierarchical modelling style and especially the top-down and bottom-up design approaches. Among the kit's elements are several types of hierarchical transitions which allow the modeller to specify the dynamics for each part of the model individually. Furthermore, a set-based type concept for predicates (places) and tokens provides for the means to model the data-flow on different levels of abstractions. Although being crucial for the interpretation of a model's dynamic behaviour, the semantics, e.g. scheduling and fairness issues, is normally not explicitly specified with a model (if at all). Therefore, one goal of this work is to enable the reader of a model to retrieve the underlying semantics of the modelling constructs used (as an option).

The second major focus of this work is the creation of a model for a procedural interface for simulation backplanes using the above mentioned modelling kit. Starting point is the (uncompleted) CFI standard for simulation backplanes as the system to be modelled with the modelling kit. The model will allow the generation of different views onto the system, such as control-flow and data-flow in different levels of detail. This hierarchical model is being realised as a hypertext document.

Currently, the elements of the modelling kit are designed and major parts of the simulation backplane interface are modelled. The formalization of the modelling kit and the generation of the different views are the major remaining activities. The research will be completed in 1996.

Design Assistance and Tool Integration:

The work on design assistance and tool integration was performed within the SYDIS (SYnthese DIgitaler Systeme) project. The main purpose of the SYDIS project is to provide a set of tools supporting hardware/software co-design and high level synthesis applications. This toolset is called CASTLE (Codesign And Synthesis TooL Environment). To facilitate homogeneous data handling for this toolset and based on this comfortable design assistance tools are integrated into JCF/SIFRAME.

The integration of the CASTLE-Tools into JCF/SIFRAME is realized enveloping the STEP/EXPRESS standard. This integration strategy has two important advantages: STEP is an industrial standard (ISO 10303: "Product Data Representation and Exchange") and the integration becomes independent from the underlying database.

The internal data representation for CASTLE tools is called System Intermediate Representation (SIR). During the report period a complete EXPRESS-Model for SIR has been defined and a prototype of an EXPRESS-to-TIDL-Generator was implemented. TIDL is

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a DDL for the JCF/SIFRAME-Database. With the EXPRESS-to-TIDL-Generator the data definitions for the initialization of the database can be automatically generated from the EXPRESS-Model. The data manipulation in the JCF/SIFRAME-Database is handled via the SDAI procedural interface which also can be generated automatically from the EXPRESS-Model. The work on a SDAI-Generator has been started during the report period. Figure 12 outlines the integration strategy in SYDIS.

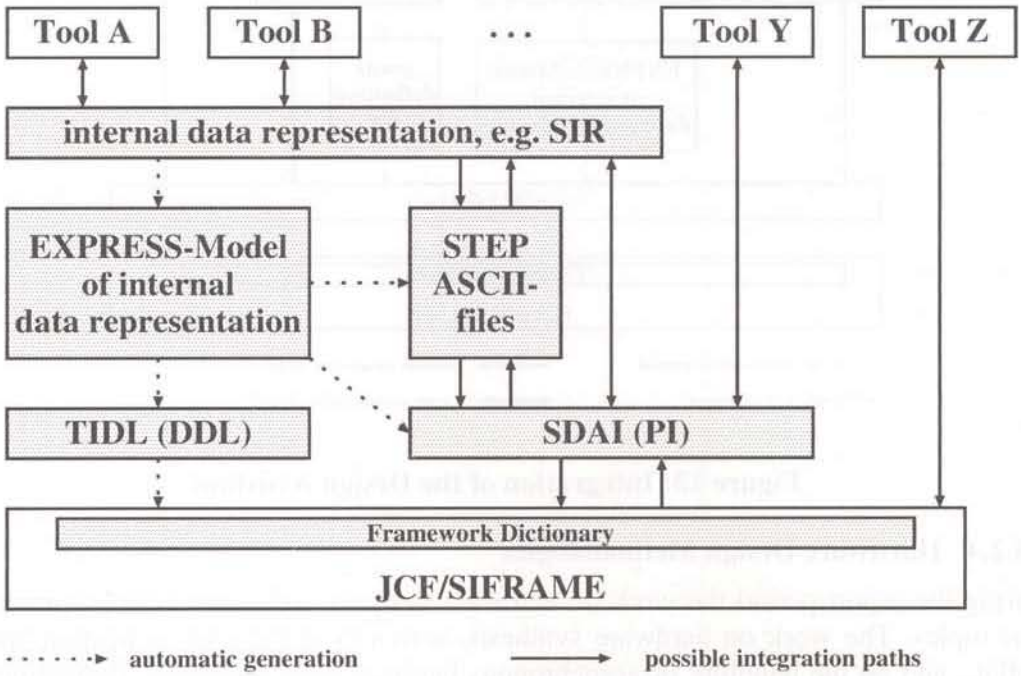

Figure 12: Integration of CASTLE-Tools into JCF/SIFRAME

During the report period an integrated design assistant was specified. The design assistant is based on extended Pr/T-Nets as underlying formal model. Possible design flows can be specified using extended Pr/T-Nets. The communication between the design assistant and the design environment is handled via events and the execution of design actions. Using events the design assistant is informed about data manipulations in the database. The manipulation of data means the manipulation of entities of the EXPRESS-Model. Transitions in an extended Pr/T-Net can be linked to the manipulation of EXPRESS-Entities (create, delete, change). These links are written in an *event definition file*. This file is read by the SDAI-Generator together with the EXPRESS-Model. Then the SDAI procedures automatically generate events when the specified data entities are manipulated and the design assistant has the possibility to update its representation of the actual design state. So the events allow the design assistant to observe the design environment. In addition the execution of design actions (tools) can be linked to the firing of transitions in an extended Pr/T-Net. Consequently, the design assistant can actively control the design flow and for example automatically invoke the execution of tool sequences. Like the integration the design assistant is based on STEP/EXPRESS to be independent from the underlying database. Figure 13 describes the integration of the

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design assistant in SYDIS.

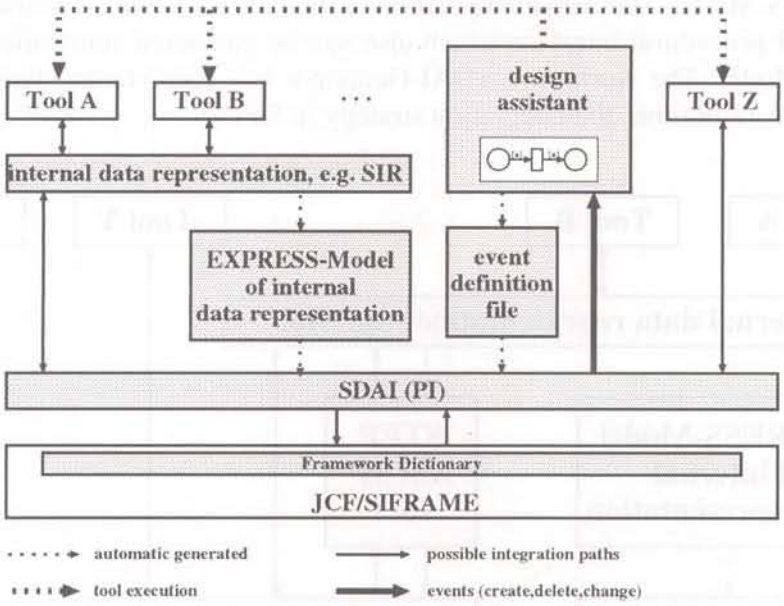

Figure 13: Integration of the Design Assistant

4.3.2.4 Hardware Design Methodologies

During the report period the work on hardware design methodologies concentrated on four topics. The work on hardware synthesis, activities in the standardization area of VHDL, and on the handling of asynchronous hardware was continued. Furthermore, a research activity on the use of formal methods for the validation of system specifications with VHDL started, which is closely linked to the other VHDL activities.

Hardware Synthesis:

The work on the project OMSI (Optimized Model Transformations at the Synthesis of Digital Information-Processing Systems) was completed at the end of 1994. In this project, Cadlab cooperated with the Technical University of Ilmenau, the Humboldt University Berlin, and the GMD. The goal of OMSI was to improve the interactions between the synthesis phases.

In a cooperation of Cadlab and the Technical University of Ilmenau, the logic synthesis tool CLASSY and the layout generator GeLaS were integrated to build a fully automatic generator of datapath layouts. At the end of the project OMSI, this datapath generator together with the high-level synthesis, controller synthesis, and layout synthesis tools developed in the project was used to perform several real designs. The results of the project OMSI were presented at a workshop in Berlin in December 1994.

Furthermore, the development of algorithms for topological compaction was completed. Experiments on a number of benchmarks showed that the use of these algorithms in the

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chip assembly leads to a reduction of the layout area of up to 10%.

Handling of Asynchronous Hardware:

During the report period the work concentrated on the synthesis of asynchronous hardware interfaces. An asynchronous realisation of interfaces has the advantage to allow the easy connection of a wide range of different hardware components without being constrained by time and speed. To improve the synthesis of hardware interfaces an asynchronous pipeline architecture was developed. Based on the investigation of different asynchronous protocols work was concentrated on the 'delay insensitive, two phase' protocol.

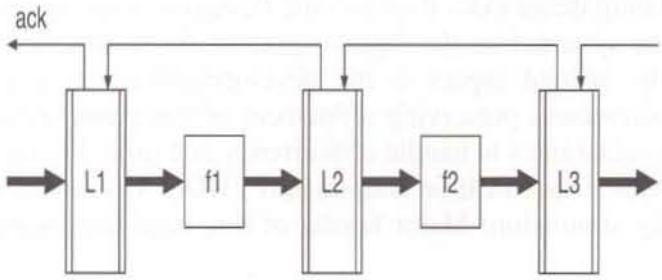

Figure 14: Pipeline with 'Delay Insensitive' Protocol

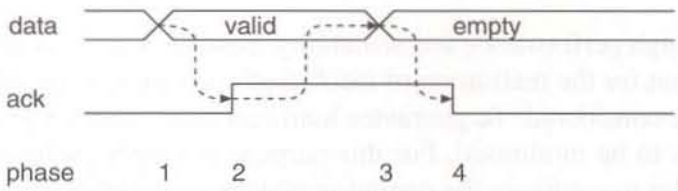

Figure 15: 'Delay Insensitive, Two Phases' Protocol

A pipeline (as shown in Figure 14) consists of latches (L1, L2, L3) and function blocks (f1, f2). The term 'delay insensitive' means that through a coding of the data itself the successing module recognizes when valid data is arriving. The term 'two phase' means that the transportation of a new data item is performed only by the change of the data value and the acknowledge. A 'return to zero' as for other protocols is not necessary. For this 'delay insensitive, two phase' protocol various cells were designed on transistor level. The cells were simulated and tested within the Cadence Design Framework 2[1]. First results encourage further study.

1. Design Framework 2 is a trademark of Cadence Design Systems.

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VHDL Activities:

The work in the standardisation area of VHDL has been continued in the corresponding work package of the European ESIP-project (EDA Standards Integration and Promotion). In cooperation with the Swedish partner Synthesia, Cadlab has worked in two main areas. The first area covers the observation of standardisation activities both in system specification and in VHDL. The second area addresses the integration of the outputs of the standardisation bodies into a common method supporting a complete design flow beginning at a specification and ending up with a VHDL program.

In 1994, a research activity has been started to combine formal methods with VHDL for the validation of system specifications. To begin with, a modelling framework based on the Z notation is being developed. It allows the designer to specify non-sequential systems (e.g., real time systems) on the highest level of abstraction using application specific packages. The second aspect is the development of an extended Refinement Calculus for the correctness preserving refinement of the given specification. The new calculus includes special rules to handle concurrency and time. Finally, the correct transformation of the refined specification is done into VHDL. This enables the validation of the specification by simulation. Major results of this work are expected at the end of 1995.

4.3.2.5 System Design Under Timing Constraints

Cadlab's activities concerning this subject are three-fold: real-time problems for the design of mechatronic systems, timing analysis for hardware systems, and project planing were regarded.

Because of their high performance and scalability massive parallel systems become more and more important for the realisation of mechatronic systems. Especially, real time conditions have to be considered. To guarantee hard real time conditions, the operating system overhead has to be minimised. For this purpose it is very useful to pre-analyse the application in order to configure the operating system. Usually, complex real-time applications involve many tasks which behave very static (i.e. their run time and their communication requirements are deterministic).

During the report period work in the field of real-time systems has focused on the design of a suitable pre-analysis tool which analyses the static processes described by the common model. Starting with the know-how of the hardware development methods *high level synthesis* and *timing verification*, research was done with respect to scheduling and allocation of periodic hard real-time tasks. As a first result a schedulability test was invented, which checks whether the hard real-time conditions are met. This schedulability test especially takes into account the problems of communicating tasks within parallel systems. The work concerning allocation will be accomplished during the next report period and became part of the BMBF-Project "METRO" starting in April 1995.

The integration of the Cadlab Timing Analysis System (CaTAS) into the EMC-Workbench was further improved during the report period by including timing information

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into the SULTAN format both for specification and back-annotation.

Cadlab's know-how in the fields of timing analysis and editor design (of the former SET-Group) was used to start designing Cadlab's project planning project CAPLAN. CAPLAN will especially allow simultaneous editing of the same project plan by different users and analysing the plan with respect to important dates (timing analysis).

4.3.2.6 Evaluation of the JESSI Common Framework

The work within Subproject 4 ('Evaluation') of the EU project "JESSI Common Frame" was continued. In 1994 at first a preliminary framework version JCF R3.0 was received. To support the quality assurance process for the final version a task force for testing was set up with both, experienced and novice users of the framework. A detailed evaluation report was written containing also quantitative measurements of the performance of the framework.

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4.4 Human-Computer Interaction - HCI

4.4.1 Baseline

Human-Computer Interaction plays a key role in the acceptance of any computer systems. Among the various aspects of human-computer interaction, the Cadlab project group HCI focuses on the graphical user interface and the development of graphical editors. Based on the know-how gained by former research and development activities in this field, the project 'Advanced Editing Systems' has been started. The main goal of this project is to transfer the research results and the know-how in developing graphical editors into industrial re-usable software systems. Furthermore, there is substantial internal requirements on an application framework for graphical editors to avoid building the same basic graphical routines for different development projects.

At the beginning of the report period, the process segment 'Problem Analysis' of this project has been completed successfully. The results of this process segment defined the requirements for the software product EOS and a prototype of the editor object system EOS. Further, two prototype applications (EXPREME and SCALOR) have been developed based on this EOS prototype. The two prototype applications showed that the basic concepts of EOS are practicable. Based on the two prototypes, the product version of EXPREME and SCALOR have been designed and developed.

Accompanying the above development activities, the group human-computer interaction oriented the research directions into the domains of visual programming and of graphical animation.

4.4.2 Work during the Report Period

4.4.2.1 Editor Object System (EOS)

Within the report period, the human-computer interaction group continued the development of the editor framework EOS (Editor Object System). The main goal of EOS is to provide an extendable, easy to use, and window system independent set of class libraries and tools, which enable the user to design and implement graphical editors. Unlike other User Interface Management Systems, EOS assists the programmer of an editor not only by providing user interface elements, like buttons, menus or scrollbars, but focuses on the drawing area part of an editor. Among the usual graphical functions, it also provides mechanism for active dialogue control with nonblocking input requests and supports a task- and semantics-oriented programming.

The first version of EOS 1.0 has been developed with SNI T30 quality both for the UNIX/Motif environment and for the DOS/Windows 3.1 environment. The main development efforts were dedicated to the Windows implementation of EOS devices. This version was also used for the development of the three graphical editors, EXPREME, SCALOR, and Pictorial Janus which will be described in the following three sections.

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4.4.2.2 A Graphical Editor for Express-G (EXPREME)

EXPREME is an easy-to-use graphical Editor for the fast design of EXPRESS-G models. The user can annotate the graphics with all non-graphical EXPRESS features. This enables generation of complete EXPRESS-Text. EXPREME is a joint development project between the IT groups HCI and DIM. Figure 16 is a screen dump of the current version of EXPREME.

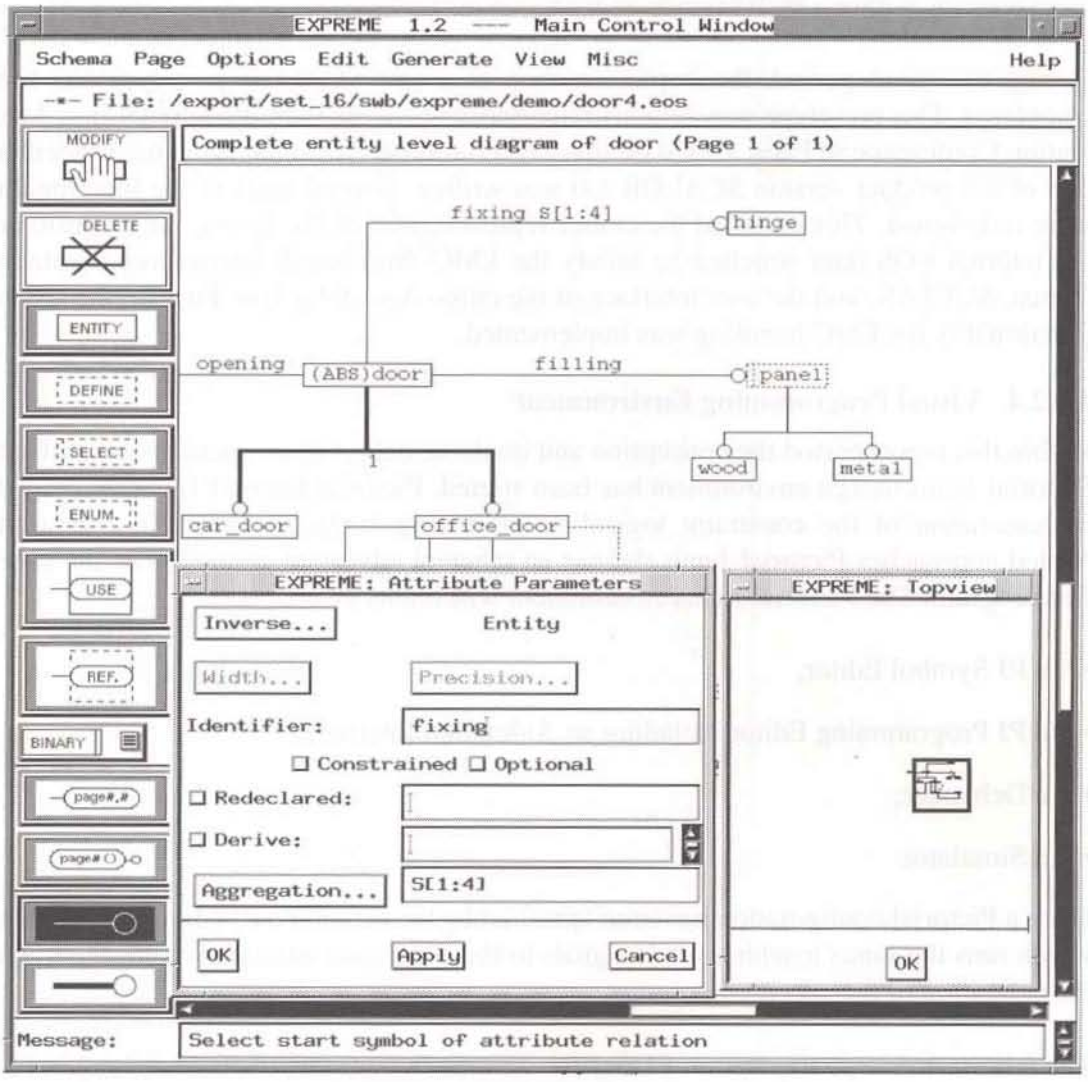

Figure 16: EXPREME-Screen Dump

EXPREME recognizes symbols on-line, prevents from drawing prohibited relationships or using reserved words as identifiers. Within the working period, a product quality version of EXPREME has been implemented. Special development effort was dedicated to the Windows version.

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4.4.2.3 A Graphical Editor for EMC-Workbench (SCALOR)

One of the development activities within the report period was the development of the editor SCALOR, which is part of the EMC-Workbench. The EMC-Workbench is used for the design and analysis of printed circuit boards under electromagnetic compatibility. Within the current EMC-Workbench, the LDA tool analyses a PCB layout for components and areas, where EMC problems may occur. Such components must be considered by corresponding EMC-arrangements. SCALOR is designed for supporting such arrangements within a PCB layout.

During the report period, the implementation of a first SCALOR prototype has been completed. This prototype was demonstrated successfully on the European Design Automation Conference in Paris. Based on this first prototype, a detailed functional specification of the product version SCALOR 1.0 was written. Several parts of the functionality were redesigned. This included the colour representation of the layers, the extension of the internal EOS data structure to satisfy the EMC-Workbench internal representation format, SULTAN, and the user interface of the cross-view definition. Further, the editing functionality for EMC handling was implemented.

4.4.2.4 Visual Programming Environment

Within this report period the conception and implementation of an interactive distributed Pictorial Janus design environment has been started. Pictorial Janus (PJ) is the complete representation of the constraint logical programming language Janus. In contrast to related approaches Pictorial Janus defines an inherent advanced animation of the specified program. The Pictorial Janus environment will finally cover

- a PJ Symbol Editor,
- a PJ Programming Editor including an Animation Interface,
- a Debugger,
- a Simulator.

Once a Pictorial configuration has been specified by the use of the PJ editor the simulator which runs the Janus machine sends signals to the animation interface in order to trigger the animation of the specified program.

The editors are implemented on EOS 1.04. The de-facto standard PVM 3.3 is used for the interprocess communication between the editor and the simulator/debugger. The software still has research status in order to investigate visual programming and debugging methodologies.

4.4.2.5 EXPRESS/EXPRESS-P

The process modelling language EXPRESS-P has been defined in cooperation with Heinz-Nixdorf-Institut, Paderborn. EXPRESS-P combines the concepts of the ISO 10303-11 data specification language EXPRESS with the concepts of the process modelling language GRAPES-86[1] and SDL[2], respectively. An active participation in the

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EXPRESS Working Group of the DIN NAM 96.4.4 provides Cadlab's contribution to the definition of EXPRESS Version 2 with the EXPRESS-P experience.

Within this report period the EXPRESS/DIS[1] checker ICE V1.0 has been implemented. The executables have been made freely available by anonymous ftp for seven different platforms (SunOS, IRIX, HP-UX, DomainOS, RS6000, OS/2, Linux). Meanwhile, the checker is well accepted for the conformance testing of EXPRESS models in the STEP community. ICE V2.0 for EXPRESS/IS will be available in the next report period.

An environment for the conformance testing of STEP Physical Files (ISO 10303-21) for the validation of huge STEP Physical Files has been investigated and implemented in the context of a diploma thesis. The validation of STEP files up to 800 MBytes has been successfully checked w.r.t. the corresponding EXPRESS specification by the parallelization of the checker under the de-facto standard procedural interface PVM 3.0. By this approach, huge physical files can be efficiently validated on a network with low-cost Sun-4 workstations.

4.4.2.6 VHDL'93

HCI has contributed to ANSI/IEEE Std 1076-1993 as a balloting member of the VHDL'93 standardization group.

A formal definition of the VHDL'93 simulator has been defined based on Evolving Algebras. This work is the first formal model of behavioural VHDL'93. The formal model has been defined in cooperation with Heinz-Nixdorf-Institut, Paderborn and University of Pisa.

4.4.2.7 Other Activities

During the first months of the report period one member of the project group continued to support the desktop development of the framework SIFRAME 3.0.

Furthermore, one member of the project group continued his work as a project consultant for another SNI department (OI 201). The project goal was to design and implement an information system for exhibitions, which was successfully installed and used at the CeBit '94. The software is based on X11, OSF/Motif and Informix.

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1. G. Held, "Sprachbeschreibung GRAPES", Siemens AG, Berlin, Germany, 1980
2. CCITT Z.100, "CCITT Recommendation Z.100: Specification and Description Language SDL (Blue Book, Volumes X.1-X.5)", CCITT General Secretariat, Geneva, Switzerland, 1988
1. Draft International Standard

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4.5 Summary and Outlook

The merger of Cadlab groups BT and SET to IT in the second quarter of 1994 has represented a major challenge for all Cadlab employees concerned. Besides continuing existing activities the expected synergy and cross-fertilisation were achieved in the areas of process and system modelling and of data integration and modelling. New application domains like transport or traffic systems have been encountered by and coped with available IT solutions. In all IT projects the momentum was kept and considerable progress has been made during the report period:

Considerable efforts were spent on the development of Intelligent Framework Services (IFS) and Predicate/Transition-Net (Pr/T-Net) tools as parts of the core environment for systems engineering. IFS represents the declarative branch of the core environment while the Pr/T-Net tools represent the operational branch. As central parts of IFS the knowledge representation and access component (KAL) and the knowledge evaluation component (KEC) were provided. For the Pr/T-Nets a data schema was designed and implemented. It covers hierarchy, the handling of sets, and timing for net structure and net behaviour. Based on this data schema prototypes of a Pr/T-Net editor and simulator were realized. In the context of the BMBF project SYDIS a Pr/T-Net based Design Assistant was integrated with the CASTLE tools employing the STEP SDAI procedural interface in order to be independent from the underlying database. As example integration platform JCF/SIFRAME has been used.

The approach pursued by the IFS project has been verified by applying the developed IFS technology in two areas: An advisory system for EMC evaluation purposes and traffic optimization employing intelligent services have been successfully demonstrated.

The work on mechatronic systems was continued. Firstly, the specification of discretized continuous system was further elaborated. Secondly, hard real time conditions, appearing when realizing mechatronic systems in a massively parallel manner, were regarded. As a first result a schedulability test for periodic hard real time tasks was developed.

In the area of data integration and data modelling progress was made in the construction of an advanced software environment for product data modelling based on the international ISO-standards "STEP" and "EXPRESS". Here, the front-end of the Cadlab STEP/EXPRESS-Workbench was successfully completed and made available to beta-users on an international scale. In the future, this workbench will be able to easily connect to a wide range of heterogeneous, distributed data bases as found in any larger company. The mechanisms for this connection have been (and are still) developed under the name "Data Base Federation, DBF". DBF addresses the requirements of data base federation, integration, migration and data independence and thus provides answers to urgent data base management problems in industry and commerce. During the report period, a demonstrator of DBF was completed and successfully piloted in the SNI factories for mid-range systems.

Concerning human-computer interaction aspects, the project on "Advanced Editing Services, AES" was carried on. A key achievement of this project was the provision of a

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comprehensive C++ library "Editor Operating System, EOS", providing classes and methods for the efficient construction of advanced platform independent editing systems. By employing EOS, the schema editor SCALOR and the EXPRESS-G editor EXPREME (both for UNIX and PC systems) have been implemented in a very fast and efficient way. SCALOR was developed together with the Cadlab group ASE and has been successfully demonstrated at DAC'94 and EDAC'94, whereas EXPREME has been delivered to a number of test sites for evaluation purposes with some first positive user reactions.

The EXPRESS/DIS checker ICE V1.0 has been implemented and its executables have been made freely available by anonymous ftp for seven different platforms.

Efforts have been spent by IT in supporting the development of SIFRAME in close cooperation with SNI BU ES CE and in evaluating and in testing corresponding results of the JESSI Common Framework project. Two releases of the framework were evaluated and tested.

From a scientific point of view IT results have been reported in numerous conference and workshop papers. In addition, numerous contributions to books and journals have been made. A book on "Handsketch-Based Diagram Editing" written by R. Zhao has been published.

The following PhD theses have been completed within IT during the report period:

- F. Buijs: "Automating the Logic Synthesis of Arithmetic-Logic-Units;
- H.-J. Kaufmann: "EDIS: Eine objekt-orientierte Software-Architektur für graphische Editoren";
- B. Kleinjohann: "Synthese von zeitinvarianten Hardware-Modulen";
- L. Kleinjohann: "Integrierte Entwurfsberatung auf der Basis erweiterter Prädikat-Transitionsnetze".

Continued applied research work was carried out in a number of areas including "heterogeneous system design", "timing analysis", "visual programming", "simulation backplanes", "data base federation", "design transaction management" and "object-oriented integration". Here, a series of PhD theses are expected to be completed in the near future.

IT members actively participated in DIN and ISO STEP/EXPRESS standardisation bodies contributing results from, among other sources, an SNI working group on STEP/EXPRESS and on its potential interworking with EDIFACT and process modelling. In addition, IT contributed to ANSI/IEEE Std 1076-1993 as a balloting member of the VHDL'93 standardization group.

Another high-light during the report period was the organisation and moderation of an ERIKA meeting by Cadlab in Paderborn in the context of European-wide activities in the area of "Knowledge Asset Management". Fruitful contacts have been established within

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this community.

Future work of IT will cover activities for the further industrialisation of EXPREME and DBF. The latter will be conducted under its new name "Open Database Middleware, OpenDM".

Work in the context of process and system modelling employing the extended Pr/T-Net paradigm together with knowledge representation means will be continued. The integration of these operational and declarative paradigms will be started. First concepts will be developed for rule-based optimization of systems described by Pr/T-Nets. The SYDIS project and the corresponding work on design assistance and tool integration for the CASTLE toolset will be completed.

The forthcoming BMBF funded project "METRO" dealing with mechatronic systems will represent an opportunity to further enhance the system modelling and evaluation approach by providing additional requirements from and by applying it in the mechatronic systems domain. The focus of this project is the use of massively parallel computers during design and realisation of mechatronic systems.

The "Global Engineering Network, GEN" initiative together with other "multi-media-keep-in-touch" efforts will give Cadlab's "traditional" work in the area of engineering environments a new push by combining Cadlab's existing middleware and integration technology with multi-media means for better (tele-)engineering support. GEN will allow the retrieval, access, and use of engineering data via Internet/WWW.

The "Product Data Management System, PDMS, Integration Project", to be run in cooperation with SNI SU MR and to be started at the beginning of the next report period, will be another chance to gain deep insights into industrial practice and needs in continuation of work done by the former TMG group in the context of the SUMR CAI project. Cadlab employees will directly work together with SU MR colleagues in their offices. From this cooperation, input for further (basic) research activities for Cadlab is expected.

The JESSI Common Frame project and hence, the evaluation work and the development of IFS and DBF within this project will be completed.

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5 Analog System Engineering

5.1 Introduction

The mission of the Analog System Engineering group (ASE) is to undertake research and development of software tools, methodologies, and strategies for design support of electronic components, modules, and systems with respect to their ElectroMagnetic Compatibility (EMC).

In recent years the work of the Analog System Engineering group was focused on the development, implementation and productization of the EMC-Workbench, an integrated environment for the EMC-adequate design of printed circuit boards. For this reason a lot of basic research in the area of wave propagation, micro wave theory, circuit theory, modelling of components and circuits, and computer science for EMC applications (e.g. placement- and routing strategies) was necessary. The EMC-Workbench consists of different tools for placement analysis, layout data extraction and pre-analysis, calculation of transmission line parameters, simulation of reflection- and crosstalk-effects, and for the simulation of radiation and irradiation phenomena. Furthermore, a tool for the comfortable graphical post-processing of simulation results and measurement data, a simple schematic and layout editor for fast trial- and error simulations as well as an EMC-device-library are included. All these tools were integrated in order to obtain a homogeneous environment which can be used by experienced as well as by unskilled users. Due to intensive contacts to and excellent cooperation with printed circuit development departments of Cadlab's industrial partner SNI a lot of experience was gained from real life industrial projects which was consequently exploited for improvement and enhancement of the software in order to obtain product maturity.

For industrial and commercial exploitation of the EMC-Workbench, a new Electronic Design Automation (EDA) company - INCASES Engineering GmbH - was founded in November 1994. INCASES took over the proprietary rights of the EMC-Workbench and is now commercializing the software. As maintenance and further-development of the software requires a lot of EMC-relevant knowledge, the major part of the EMC-Workbench development team moved to INCASES and is still closely cooperating with the Analog System Engineering group. This spin-off is an excellent example for the exploitation of Cadlab's R\&D results and marks a significant milestone in Cadlab's history.

The new objective of the Analog System Engineering group is the development of tools, methodologies, and strategies for the EMC-adequate design of entire electronic systems.

5.2 Baseline

During the design of electronic components, subsystems (modules), and systems physical effects of thermal, climatic, mechanical, as well as of electromagnetic origin have to be taken into account in order to be sure that the system to be developed meets all

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requirements after manufacturing. Especially the ongoing complexity, miniaturization, integration density, and processing speed of any electronic equipment, which are necessary to provide the required performance and low production costs, lead to an increasing sensitivity with regard to electromagnetic interference. All effects and disturbances of this origin and all measures which are necessary to reduce or minimize the effects or their consequences, are covered by the term ElectroMagnetic Compatibility (EMC). EMC-effects (e.g. reflection, crosstalk, current spikes, delta-I-noise, electrostatic discharge, radiation, etc.) may cause malfunctioning on component-, subsystem-, and system level. These interference effects are no separately occurring phenomena, but they have to be considered as significant properties of a particular design and therefore, EMC-effects are design relevant subjects. Targeting at a sufficient functionality of the entire system, the development- and design process has to consider EMC-aspects and given EMC-standards. Among these functionality aspects also the security and quality of electronic products may strongly be influenced by EMC-effects and national as well as international regulations (e.g. European Community Council Directive 89/336/EEC) were set up. Moreover, European EMC-requirements (CE-conformity) will force designers to apply EMC-adequate design and analysis methods to the various design stages as early as possible. EMC-problems cannot be solved by conventional design methods because the already increasing integration densities at all design levels lead to difficulties in detecting EMC-effects by measurement taking also into account general restrictions of measurement procedures due to costs, possibilities as well as development-time constraints.

Considering these technical and economical requirements the development of software tools, methodologies, and strategies for the EMC-adequate design of electronic systems becomes very important. Currently the major part of the functionality of an entire system is mostly provided by printed circuit boards which are therefore of special interest. These modules or subsystems can be designed EMC-adequate using the EMC-Workbench, which was developed in recent years. After this first and successfully reached milestone the development of appropriate tools and methodologies for the EMC-adequate design of entire systems is the objective of the Analog System Engineering group. For this reason a lot of experience and knowledge gained during the development of the EMC-Workbench will be transferred to this extended problem area. This means that new methods and algorithms will be developed and already existing ones will be improved and further developed in order to meet the enhanced demands resulting from the analysis of entire systems. Due to the complexity of this task the global objective has to be subdivided into partial ones. For this reason the future work focuses on five main topics which are given below.

- Tools and Rules:
  Development of algorithms (e.g. for characterization of transmission lines, simulation of conducted wave propagation, etc.), simulation tools, and pre- and post-processing tools as well as rules for a correct application of the simulation tools.

- Numerical Field Computation and Application:
  Development of methods, algorithms, and software tools for the simulation and analysis of radiation caused by complex systems and subsystems. Furthermore, the development of appropriate measurement methodologies using field scanners and TEM

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and/or GTEM cells for the validation of simulation results as well as for combined measurement-simulation analysis methodologies belong to this task.

- Modelling:
  Development of models for digital and analog components and integrated circuits as well as for modules. Furthermore, the development of modelling strategies and tools or environments for an (semi-)automatic generation of macromodel-structures are important subjects within this area.

- Rule Based Advisory System:
  Development of design rules, strategies for their application, and appropriate advisory system components for the support of an EMC-adequate design of systems and subsystems.

- System Design:
  Development of the System-Workbench, which requires the results of all main tasks mentioned above. Furthermore, the modelling of design processes, development of strategies for system design and system planning are main subjects of this area.

These working areas can be defined as the basic fundamentals for the EMC-adequate system design and they will also be the basis for the necessary restructuring and new adjustment of Analog System Engineering.

5.3 Work During the Report Period

During the report period work focused on two main topics. The first one was the further development of the EMC-Workbench for EMC-adequate design of printed circuit boards and the application in industrial application projects.

Secondly, the work was concentrated on first investigations of basic fundamentals in the area of system design. The concept of the Microsystem-Workbench, described in the previous annual report was further developed in order to obtain the basis for an overall System-Workbench. In this frame a generalized design process has been defined which can be used to illustrate and model the design- and development process of arbitrary systems, microsystems included. In order to start optimizing the EMC-behaviour of a system already during the planning phase, an EMC-optimization model has been developed which can be integrated into the generalized design process mentioned above. As the accuracy of simulation of electromagnetic interference effects depends significantly on the quality of available simulation models for components and modules, a lot of effort has been spent in developing appropriate (semi-)automatic methods and procedures for the generation of macromodel structures and their parametrization. In the area of rule based advisory systems the experience and knowledge gained from EMC-adequate design of printed circuit boards was used to define and to develop an EMC-review process which consists of different characteristic phases. This review process will be the basis for the future research and development activities in the area advisory systems.

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5.3.1 EMC-Workbench

5.3.1.1 Functionality and Structure

The EMC-Workbench consists of a set of tools for the analysis of EMC-problems on printed circuit boards. The EMC-Workbench operates as a general superior tool and provides the following functionalities:

- Placement analysis,
- Layout data extraction and rule-based layout analysis,
- Simple schematic and layout editor for fast trial- and error simulations,
- Calculation of transmission line parameters,
- EMC-macromodel library,
- Reflection- and crosstalk analysis,
- Simulation of radiation and irradiation effects,
- Interfaces to different layout systems,
- Integrated, open environment.

With regard to the large number of EMC tools, the complexity of the tools and the analysis and design task itself, and the amount of opportunities to perform an appropriate EMC analysis, the user of EMC analysis software needs support in order to process the design and analysis tasks successfully and in an optimal way. This support is given by the EMC-Workbench. It provides the user with a framework and an analysis-flow shown in Figure 17, that allow an easy handling of the integrated tools and the generated data. Additionally, it prevents an incorrect or inappropriate usage.

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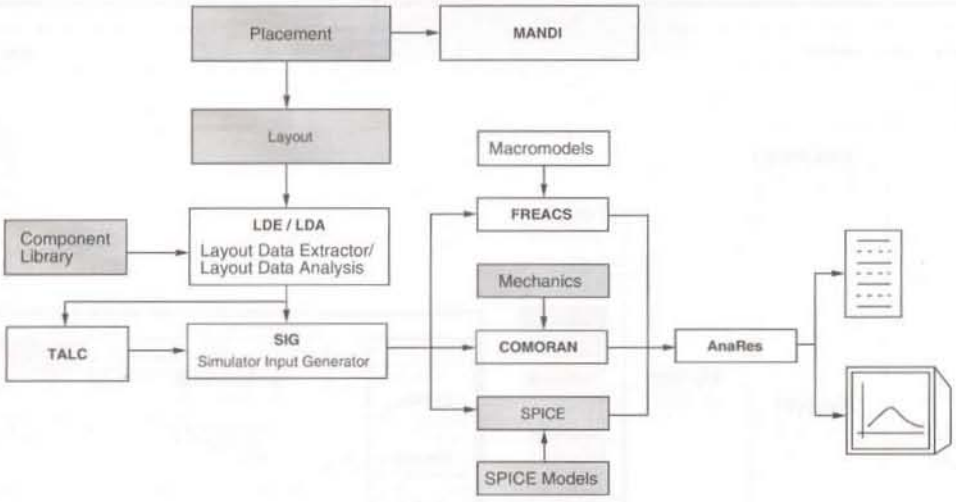

Figure 17 : Structure of the EMC-Workbench

The user-interface of the EMC-Workbench is represented by an ergonomically designed graphical desktop (Figure 18). The major dialogue-objects are popup-menus, formulas, and command buttons. The EMC-analysis flow and the respective result versions are presented by the desktop of the EMC-Workbench. In the following the functionality and the tools of the EMC-Workbench are described in detail.

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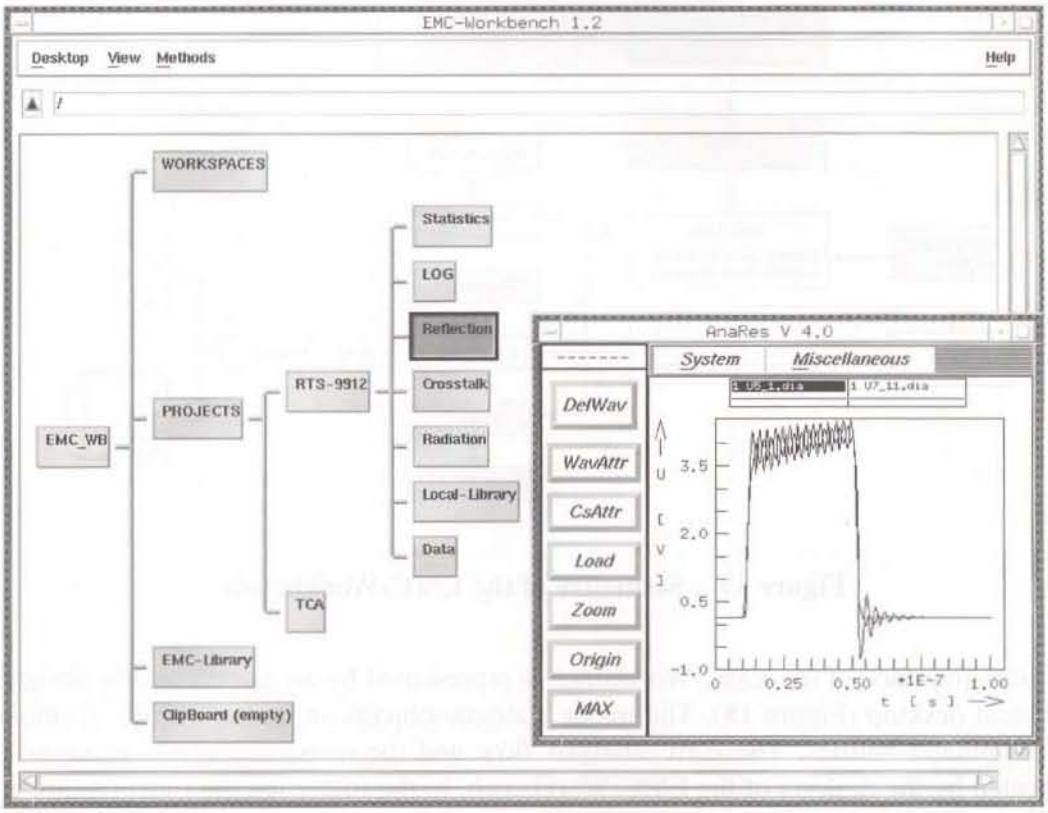

Figure 18 : Desktop of the EMC-Workbench and a Simulation Result

5.3.1.2 Perennials of placement data considering EMC-aspects

MANDI enables a fast pre-analysis of the component placement with regard to the expected net-lengths and the corresponding signal-delays. Moreover, a pre-analysis of reflection effects is offered. The description of the placement to be analysed is performed using the **SULTAN**-format which is an ASCII-format describing all EMC relevant PCB-data. SULTAN is also the basis for all further layout-analysis steps within the EMC-Workbench. The results of this pre-analysis are structured in lists and diagrams which can directly be integrated into the corresponding project documentation.

With the aid of MANDI two-point-connections, (one input/ one output) as well as any multiple-point-connections can be analysed. The length- and signal-delay approximation is based on Manhattan-Distances (orthogonal projection) as illustrated in Figure 19. Hereby, an optimal chain routing is assumed for the analysis of multi-point-connections. Passive adaption and termination networks can also be considered. The reflection analysis of two-point-connections is based on an approximation of the expected voltage amplitude concerning under- and overshoot. Hereby, the output-resistance of components, the characteristic impedance of the connecting transmission lines as well as passive circuits are considered.

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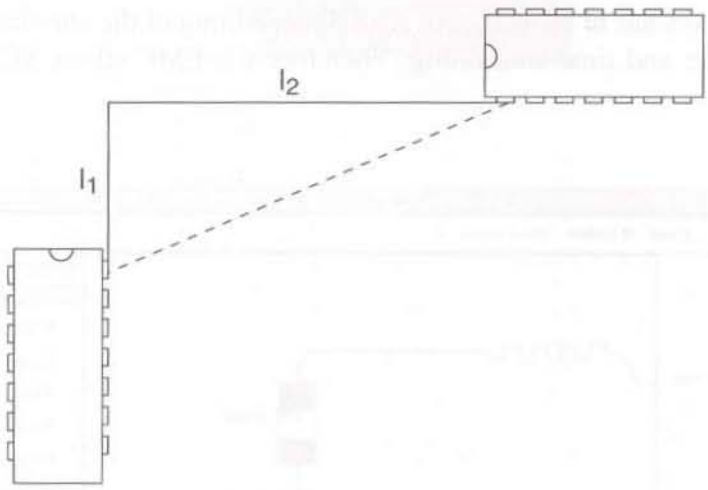

Figure 19 : Manhattan-Distance of a two-point-connection

5.3.1.3 Layout data extraction, analysis and generation of simulator input

The task of the **L**ayout **D**ata **E**xtractor (**LDE**) is to provide geometric relations between all objects of a printed circuit board layout (pins, vias, transmission lines, layer, etc.). **LDE** provides the neutral interface **SULTAN**. Every commercial available layout software can be adapted to this interface.

During the **L**ayout **D**ata **A**nalysis (**LDA**), the layout is pre-analysed with regard to reflection- and crosstalk effects. Thereby, among others, line lenghts (in dependency of the technology of the driver and the parameters Z_D and v_{ph}) as well as spacing and coupling-length of transmission lines are compared to technology-dependent critical limits. The goal of this pre-analysis is the classification of the layout into critical and non critical transmission lines. Critical transmission lines are then analysed more thoroughly with appropriate simulation programs.

With the help of the **S**imulator **I**nput **G**enerator (**SIG**), the extracted layout data are prepared for simulation. Thereby, critical transmission lines as well as sections selected by the user, can be analysed in more detail.

5.3.1.4 SCALOR - Schematic and Layout Editor

The examination of printed circuit boards with regard to EMC-problems by simulation of single critical nets often requires the construction of a non-critical EMC-solution iterative. Also, certain EMC-measures have been applied to the net under examination. A new simulation has to be started with these modified net data. These actions have to be repeated iteratively until the net shows the wanted EMC-behaviour. Using a complete schematic and layout system, this iteration would take up too much time because the

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whole PCB always has to be analysed. Also direct editing of the simulator input file is to much complicate and time-consuming. Therefore the EMC-editor SCALOR has been built.

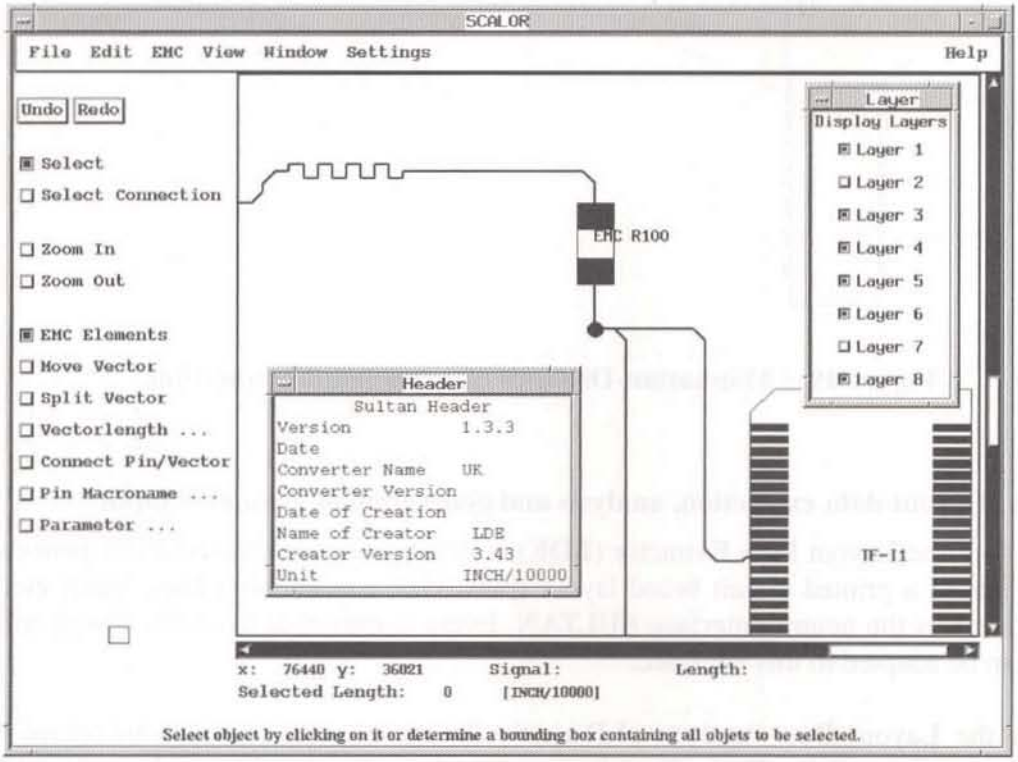

Figure 20 : User interface of SCALOR

This editor contains the most important schematic and layout editor functionalities which are accessible by an ergonomic designed user interface. Essential EMC-measures that can be easily realized by **SCALOR** in single or coupled nets to reduce crosstalk and reflection problems are for example:

- insertion/change of components (resistance, capacitor, diode, driver, receiver),
- movement/extension of transmission lines,
- modification of component and pin parameters (macromodel name and type, resistance or capacitance value, etc.),
- change of the layers of transmission line vectors,
- change of geometrical transmission line parameters (width, length),
- change of layer structure parameters (substrate height, copper height or $\in_r$).

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The input-data format of **SCALOR** is **SULTAN**. After editing or modification, the new layout-configuration again will be stored as a **SULTAN** file.

5.3.1.5 Calculation of transmission line parameters

The calculation of transmission line parametersis is performed by **TALC**, which calculates the electrical parameters (capacitance and inductance per unit length) of single and coupled transmission lines (microstrip system line- or multilayer structures).

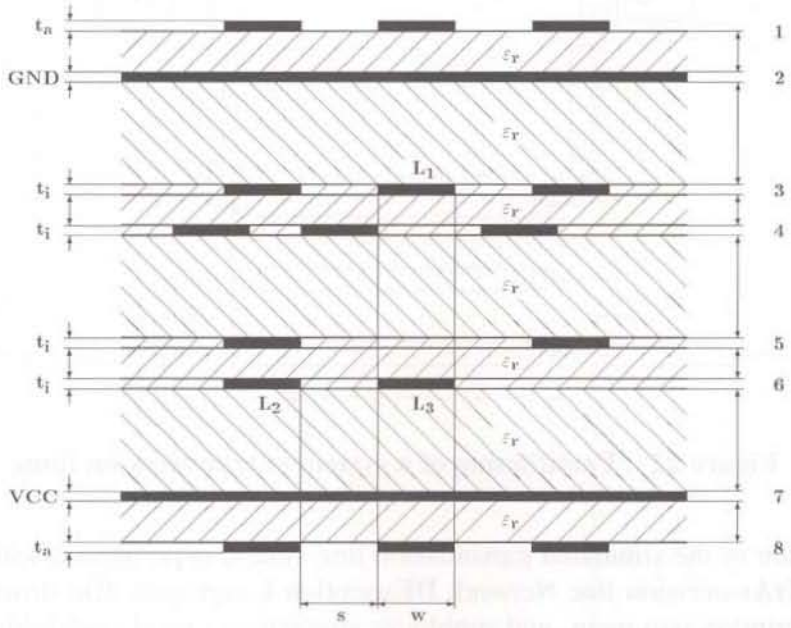

Figure 21 : Cross-section of a printed circuit board

The calculated parameters are required for the signal-integrity analysis of transmission lines using the simulator **FREACS**. The numerical algorithm is based on the Boundary-Element-Method which is used to solve the Laplace-Equation which describes the problem without significant loss of accuracy if quasi-TEM wave propagation can be assumed on the transmission lines. For applications in multilayer-technology, transmission lines within materials of different dielectric properties can be analysed. Thereby, the influence of various material conditions of different layers on the electric characteristics can be determined. The layer geometry and the substrate conditions are described by a special input language. Within the EMC-Workbench, the necessary input data for **TALC** are automatically generated. The cross-section of transmission lines can be given by any closed polygonal connection. In this way, the effects of production tolerances on the electric characteristics of the respective transmission lines can be determined. Additionally, the geometrical parameters for a layer definition with constant characteristic impedances (controlled impedances) of all signal lines can be determined by **TALC**.

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5.3.1.6 Simulation of reflection and crosstalk effects

The simulator **FREACS** supports the analysis of the transmission line behaviour of complex circuits and systems on printed circuit boards. The simulator enables an efficient analysis of reflection- and crosstalk-effects considering the non-linear characteristics of terminations.

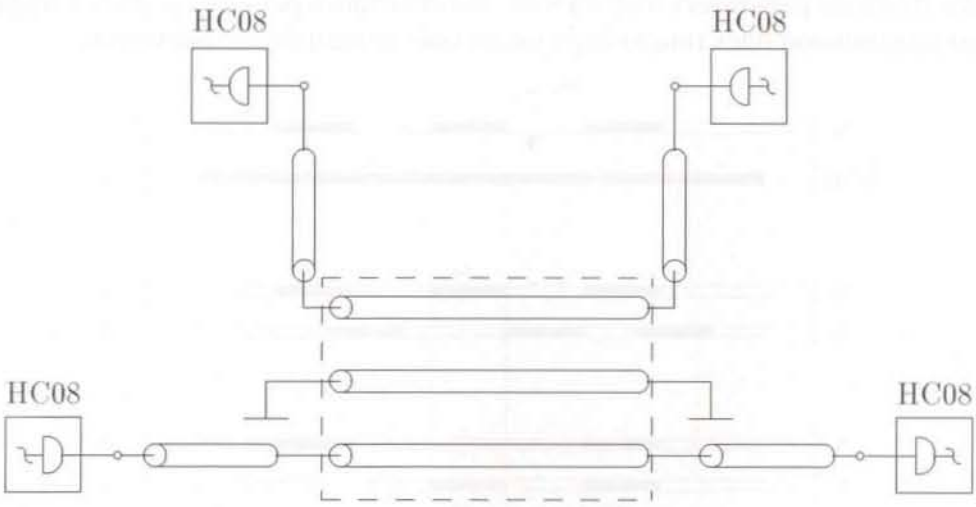

Figure 22 : Partitioning of a system of transmission lines

The description of the simulated transmission line system is performed with the help of **TANDEL** (**T**r**A**nsmission line Network **DE**scription **L**anguage). The structuring of the network description into main- and subblocks guarantees a good readability. Within the EMC-Workbench, the **TANDEL**-Script is automatically generated from the layout data. With the help of **FREACS**, lossy as well as lossless coupled transmission line systems can be analysed. Furthermore, it is possible to consider different linear and non linear components during the simulation. Macromodels, which are especially developed for this simulator, are referred to for the modelling of digital components. They describe the non linear characteristics of these components. Discontinuities, e.g. bends, vias, etc. can be considered by quasi-static descriptions. A special simulation algorithm enables an optimal adjusted step size for the evaluation of all circuit-, termination-, and discontinuity areas. With a circuit partitioning it is furthermore possible to calculate areas with only linear elements with a fast linear equation method. Due to these special characteristics, **FREACS** needs far less computation time than comparable simulation programs.

5.3.1.7 Macromodel-Library

For the simulation of reflection- and crosstalk effects on transmission line systems including circuits with a non linear behaviour (e.g. digital components), ordinary simulators (**SPICE**, etc.) need a high computation time because in general the description of the components is very complex. The numerical effort can be reduced enormously, if the terminations are described by appropriate macromodels. These models provide a simple,

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but sufficiently exact description of the input-and output behaviour of (digital) components.

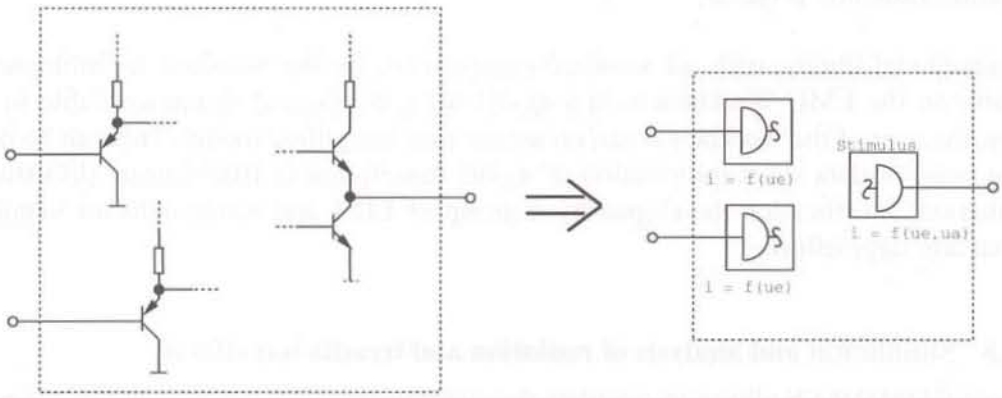

Figure 23 : Macromodel representation of digital inputs and outputs

The macromodels used by **FREACS** describe the behaviour of the components with regard to the static and dynamic input behaviour (input model) and the static and dynamic output behaviour (output model). Thus, the transient behaviour of the non linear components is described in detail.

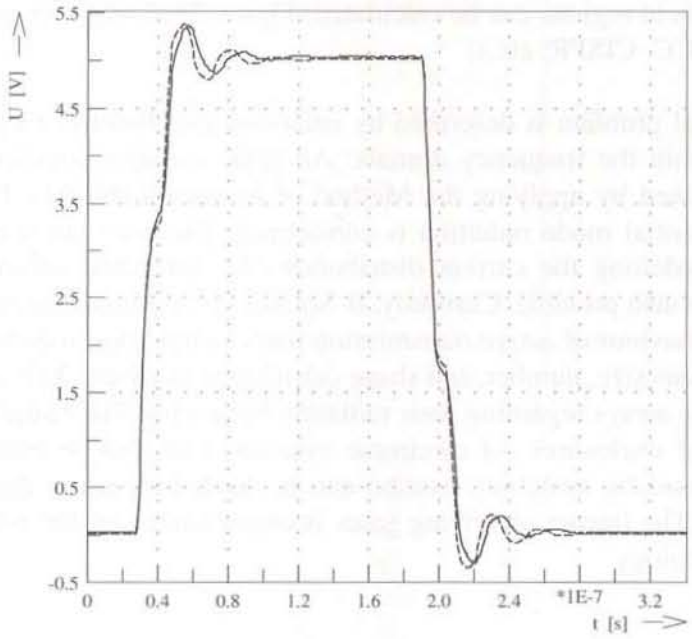

Figure 24 : Model verification by measurement

Figure 24 shows the simulation result of a macromodel representing a driver module in

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HCT-technology in comparison with corresponding measurement results. The parametrization of the models was made using measurement techniques as well as SPICE-based simulations. The quality and accuracy of the models was validated by various applications and evaluation projects.

A macromodel-library with all standard components for the standard technologies is available in the EMC-Workbench. If a model for a component is not available in the library, the user of the workbench can create his own simplified model. This can be done on the basis of data sheet information or model description in IBIS-format (I/O Buffer Information Specification developed by a group of EDA and semiconductor vendors) without any large effort.

5.3.1.8 Simulation and analysis of radiation and irradiation effects

The tool **COMORAN** allows to calculate the electromagnetic behaviour of three-dimensional transmission line structures. Additionally, conducting planes of finite size (i.e. GND/VCC-planes) can be taken into account. By application of this tool the engineer is able to check and remove violations of the legal requirements (EMI/RFI limits) before prototyping the actual printed circuit board.

In a first step during a simulation run, the necessary parameters are set up (geometrical data specification, excitations) before the current distribution of all conducting areas is calculated. For example, by means of the current distribution a reflection and crosstalk analysis can be carried-out. Then the electromagnetic fields for any observation point of the near and far field regions can be calculated (Figure 25) and compared with the given standards (e.g. FCC, CISPR, etc.).

The mathematical problem is described by means of the 'Electric Field Integral Equation' (EFIE) within the frequency domain. An approximative solution of the integral equation is obtained by applying the Method of Moments (MOM). By this, common mode and differential mode radiation is considered. The user can select various basis functions for modelling the current distribution. An automatic selection of optimum basis functions is also possible. Currently, B-Splines up to third degree are implemented. The radiation behaviour of active transmission lines located near a conductive wall with apertures of various size, number, and shape can also be analysed. This allows an optimization of aperture arrays regarding their radiation behaviour. The radiation through arbitrary apertures of enclosures (of electronic systems) can also be examined. Transient signals (e.g. caused by switching events) can be treated by using the inverse Fourier Transformation. The impact of driving gates is characterized by the typical rise time of the applied technology.

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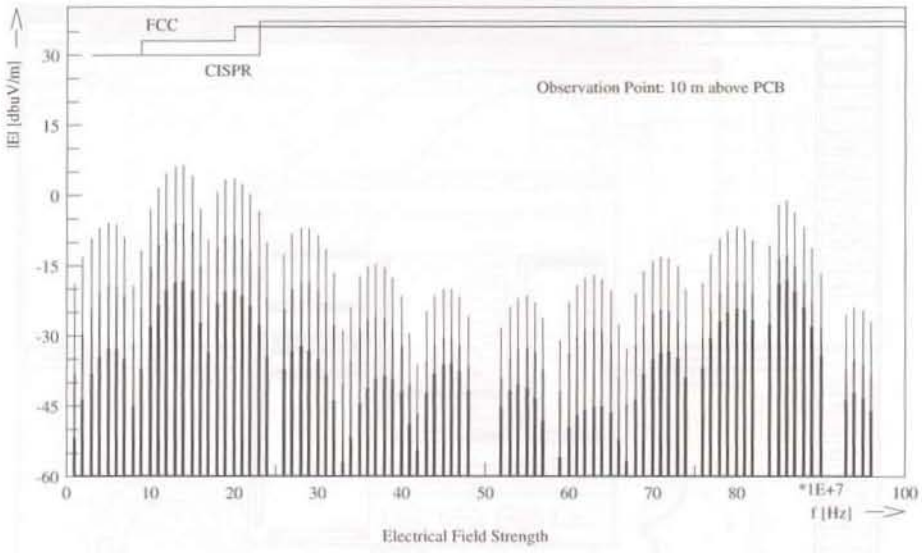

Figure 25 : Spectrum (magnitude) of the cartesian components of the electrical field strength caused by a transmission line system on a printed circuit board and FCC/CISPR limits $|E_x|$: ▬, $|E_y|$: ▬, $|E_z|$: —

5.3.1.9 Graphical representation and post-processing of simulation results and measurement data

Due to the diversity and large amount of data which accumulate during the design and simulation of systems, modules, and components, it is necessary to process them with graphical methods in order to be able to provide an accurate data analysis. For the acceptance of such tools it is inevitable to provide an ergonomic user interface, that is similar to the usual environment (e.g. oscilloscope) of the designer or engineer, respectively. These requirements are fulfilled with the tool **AnaRes** which is based on X-Windows. It is used for the presentation and analysis of data which are created by technical and scientific application software. Furthermore, the analysis of measurement results is possible. The tool offers a diversity of presentation and processing options. The arrangement of the diagrams is done according to DIN. In addition to the representation of data in form of curves, an analysis can be made by applying mathematical operators. An ergonomically designed graphical desktop is available as a user interface. The main dialogue objects are popup-menus, formulas, and command buttons as well as the actual diagram objects (axis, curves, text elements). The interface can be adjusted to the specific needs of the customer with the help of various configuration options. **AnaRes** supports the processing of input data in CSDF (Common Simulation Datafile Format) and in ARDF (AnaRes Datafile Format for any structured data). A postscript interface is implemented for the output of diagrams. The postscript output can be printed or archived for further documentation.

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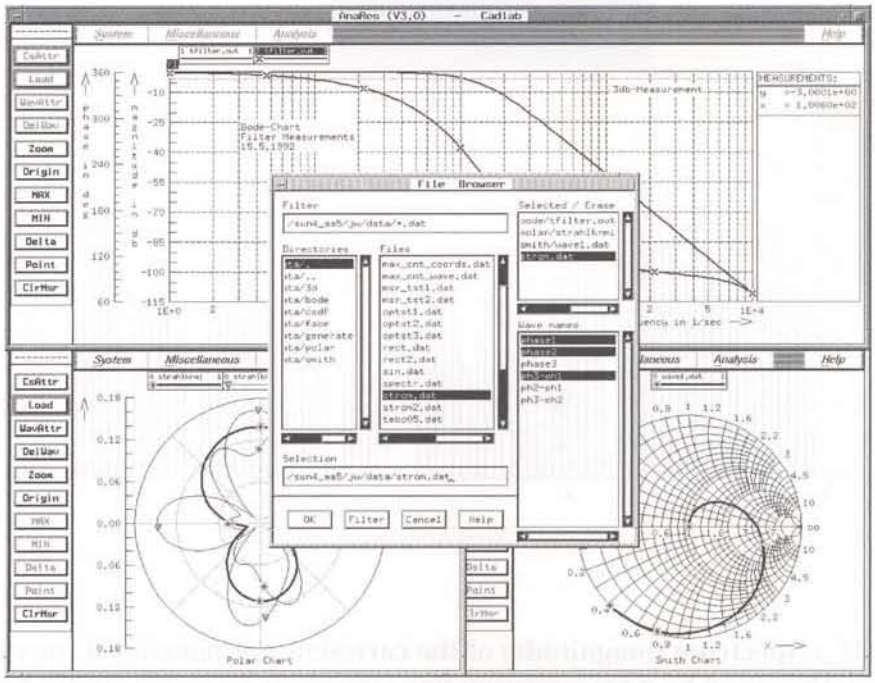

Figure 26 : User interface of AnaRes

Framework - Integration of the EMC-Workbench

The integration basis of the EMC-Workbench is composed by using the development kit of CAX framework **SIFRAME** which is based on the JESSI Common Framework **JCF**.

The user interface consists of a desktop which is set up according to modern technology. The user operates on this desktop with icons, popup- and pulldown-menus. The input can alternatively be done by command buttons or function keys (expert modus). The desktop can individually be adjusted to the specific needs and wishes of the user. The variety of the managed information is clearly presented by an advanced window technique. The set-up and the presentation of all structures is done graphically. Thereby, the overview of the EMC-analysis (projects) is improved. The current status of a project is available at any time. The design management allows

- the integration of SW-products and applications in various forms,
- the management of data communication among the different tools,
- the administration and management of design flows and
- the display of the development status of a project.

The object-oriented database-management component (OMS) provides the consistency,

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security, and no redundancy of all data. The data transfer between the framework and the applications is guaranteed by this component.

5.3.1.10 Application Example

The usage of the EMC-Workbench is shown by the analysis of a clock signal line with regard to reflection and radiation.

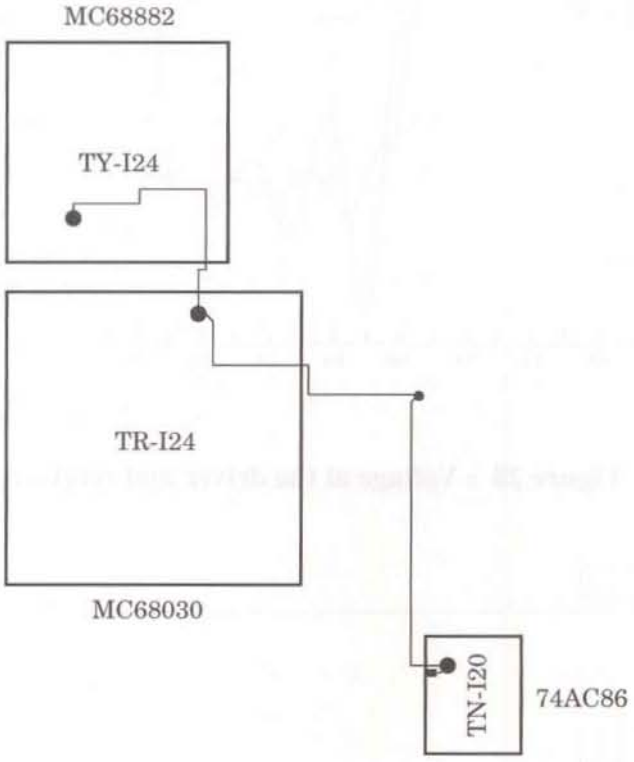

Figure 27 : Topology of the examined net

With the Layout Data Extractor (**LDE/LDA**), all EMC-relevant data (component information, geometry of the lines, layer definition, vias, etc.) and the physical set-up of the respective printed circuit board are extracted from the entire layout data. Subsequently, the pre-analysis of the extracted layout data is carried out with regard to lengths. During this pre-analysis, the arrangement presented in Figure 27 is recognized to be critical. This net consists of a driver (74AC86), two receivers (MC 68 030, MC 68 882), and several transmission line areas with different characteristic impedances and phase velocities.

During the following step, the characteristic impedances and the phase velocities for these transmission line areas are calculated with the tool **TALC**. After this, the corresponding **FREACS** input data file is generated with the help of the **S**imulator-**I**nput-**G**enerator (**SIG**). The results of the simulation with **FREACS** for the respective arrangement are shown in Figure 28. A significant overshoot and undershoot is visible. They are

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caused by the impedance mismatch of the driver and receiver to the characteristic impedance of the transmission line.

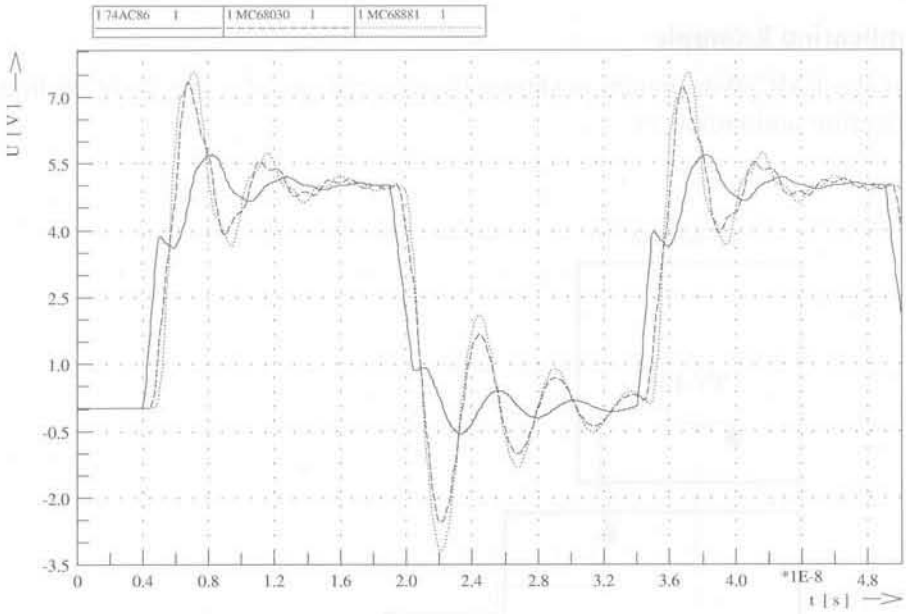

Figure 28 : Voltage at the driver and receivers

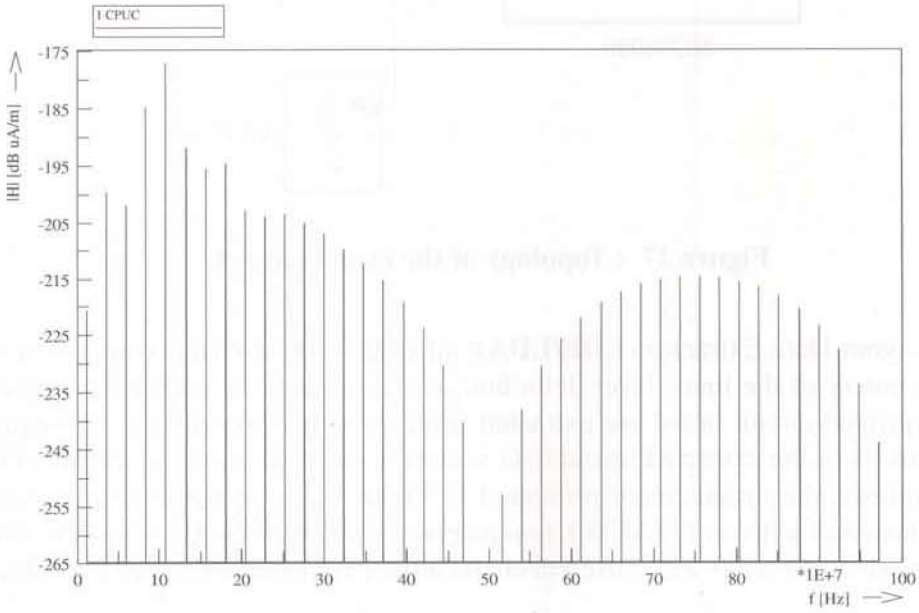

Figure 29 : Spectrum (magnitude) of the magnetic field strength

The spectrum of the magnetic field in a distance of 10 metres from the respective

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arrangement is shown in Figure 29. This result was achieved with the tool **COMORAN**.

For a reduction of the undesired reflection effects on the clock net, a serial resistor of 47 Ω is inserted directly to the output of the driver 74AC86 in order to improve the matching of the output to the transmission line. Figure 30 shows the relevant reduction of the reflection effects.

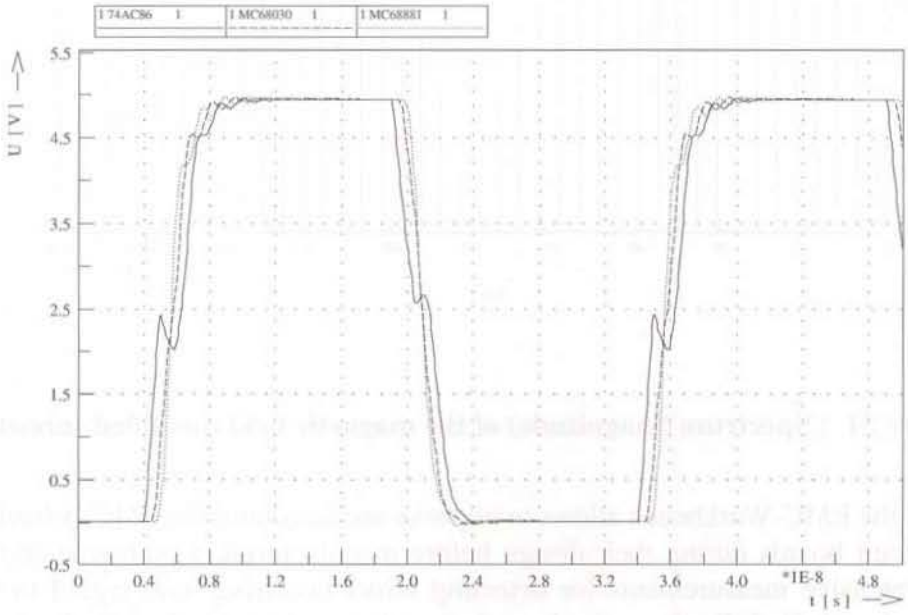

Figure 30 : Voltages of the modified subnet

The spectrum of the magnetic field is also influenced by the serial resistance. The maximum is reduced by approximately 20 dB $\mu A/m$ (see Figure 31).

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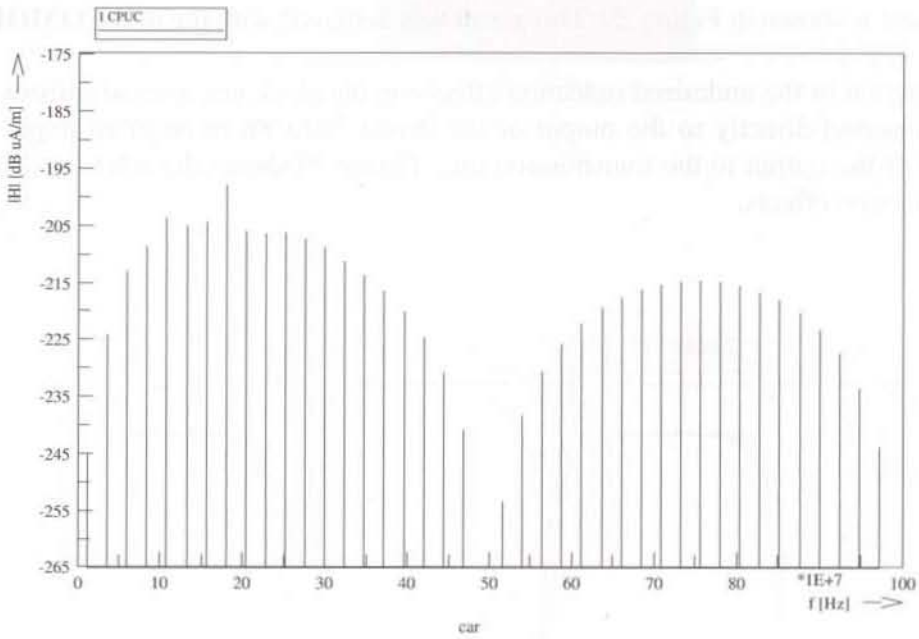

Figure 31 : Spectrum (magnitude) of the magnetic field (modified subnet)

The use of the EMC-Workbench allows to improve and to control the EMC-behaviour of printed circuit boards during their design before manufacturing a prototype and time- and cost intensive measurements for detecting errors occurring with regard to EMC-effects can be avoided. Furthermore, by reducing the number of redesigns the development time (time to market) of the product is reduced, which leads again to a significant reduction of costs and to competitive advantages.

5.3.2 Application of the EMC-Workbench for EMC-Adequate High-Speed Board Design

During the current report period various projects of the SNI development departments were supported. A lot of projects dealt with the analysis of the signal integrity (timing, reflection and crosstalk behaviour of electrical nets) of typical and/or standard arrangements used on high-speed printed circuit boards of midrange systems. The expression high-speed means the application of new and fast technologies (e.g. low voltage technology) which allow on the one hand the required performance but which are extremely sensitive against any electromagnetic interferences and their effects on the other hand.

Typical examples of investigated arrangements were backplanes, data-buses, and memory modules. These configurations were analysed in order to improve and optimize the signal behaviour of critical or sensitive nets (e.g. clock lines). The investigations were based on simulations which were partially validated by measurements. The results were

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used to set up design-rules and guidelines for the placement and routing process and for the generation of optimization measures for concrete signal integrity problems on printed circuit boards. Here, a lot of improvements to be realized by additional matching terminations and/or layout modifications could be suggested. During the analysis the dynamic input and output behaviour of the components were taken into account by the set up of appropriate models for the used components. This modelling effort was necessary because a lot of components on high-speed printed circuit boards are company specific and therefore, they are not included in the macromodel-library of the EMC-Workbench. Furthermore, the operating mode of coupled nets (unidirectional or bidirectional switching mode) were taken into account in order to guarantee an error free operation also under worst case conditions.

Besides these application areas also rules and guidelines for the definition of the layer structure for controlled impedance printed circuit boards were generated. This task was executed by a tolerance analysis, which was based on a variation of different geometrical parameters of the cross-section of a printed circuit board. By this, detailed instructions for PCB manufacturing could be generated.

These application projects aimed in two directions. On the one hand the productivity of the SNI development departments could be improved and on the other hand the experience gained from the tools application could be used to improve them with respect to their handling and their application area. Furthermore, the analysis and design flow, represented by the data-scheme of the EMC-Workbench, could be checked and significantly improved.

5.3.3 EMC-Adequate System Design

EMC-adequate system design means to consider the EMC-behaviour of the system to be developed during all stages of the design process. Within this context the term system is used as a synonym for any electronic equipment. It may contain of subsystems that are connected via arbitrary transmission systems. The following description will mainly concentrate on EMC-problems caused by conducted interference on systems level. The work focuses on the integration of an EMC-optimization model into a generalized design process. During this description the model of EMC-optimization and the necessary support- and simulation tools are explained. In the beginning there will be a global description of the general design process. In a second step the coupling of the EMC-optimization process to the generalized design process will be described.

5.3.3.1 Generalized Design Process

The design of technical systems can be mapped onto a generalized design process. In the vertical direction of Figure 32 the design process divided into characteristic design stages is shown. Additionally, the division of a system into subsystems and components is illustrated in the horizontal direction. It appears as a recursive structure with an arbitrary number of partitioning levels, each beginning with the requirement description and ending with the system test. All design stages may be passed in several iteration steps. A

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following stage can only be reached if the results of the previous one are sufficient enough to continue. In case, that the results are insufficient, one of the previous design stages has to be reviewed once more with modified parameters. In this way, different versions can be developed within one design stage. The interactive optimization covers the top-down as well as the bottom-up methodology of a design process.

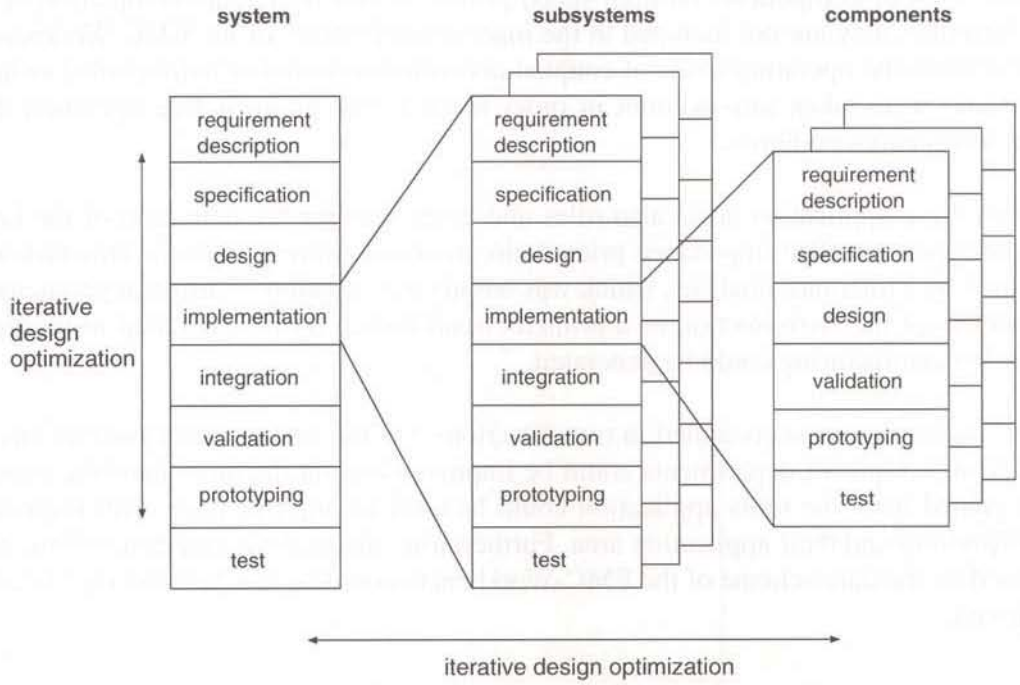

Figure 32 : Generalized Design Process

5.3.3.2 Model of EMC Optimization

The model of an EMC-optimization and it's mapping to the general design process is shown Figure 33. On the top level the model is divided into the EMC-system planning and EMC-validation. It seems to be practical to make a further partitioing of the EMC-system planning into the areas objectives/results and activities. Within the area objectives/results EMC-relevant conditions and characteristics of the system are determined. Moreover, the EMC-concept and integration proposals are described. The activities of the EMC-planning area contain a collection of procedures to achieve the objectives/results (e.g. selection of the requirement according to EMC-aspects, system pre-analysis, etc.). In this area the support- and analysis tools are integrated.

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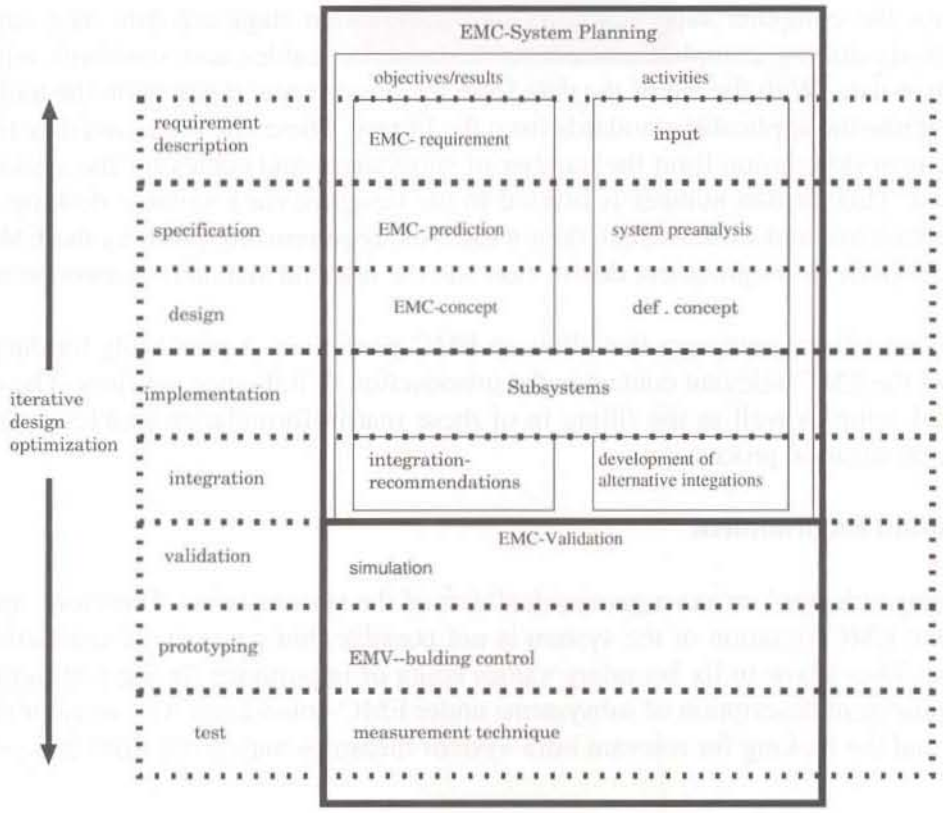

Figure 33 : Model of EMC optimization

5.3.3.3 Tools & Simulation Environment

The support tools and simulation environments needed for the first three design stages (requirement-, specification-, and design stage) are described in a rough structure.

5.3.3.4 Computer Aided Requirement Description

The major task of a tool for the structuring of EMC-requirements is the setup of EMC-relevant data from the clients order. This can be done by graphical desktop formularies. The structure of the desktop formularies are similar to the attribute hierarchy of an EMC-check list.

5.3.3.5 Computer Support within the Specification Stage

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Basis for the computer support during the specification stage are data base supported libraries describing complete choices of subsystems, cables and standards with their respective data. With the aid of the data from the requirement description the tool is able to determine the applicable standards from the library. These standards and data from the requirement description limit the number of subsystems and cables for the system to be designed. This limited number is offered to the designer via a suitable desktop. In this way subsystems and cables which do not meet the requirements given by the EMC-relevant data from the requirement description and the relevant standards cannot be chosen.

Moreover tools are necessary that allow an EMC-prediction. A possibility for the presentation of the EMC-relevant context is the introduction of influence matrices. The computer aided setup as well as the filling in of these matrix-formularies enables an efficient EMC-optimization process.

Simulation Environment

In the stage 'design' no exact geometrical data of the system exists. Therefore, an analysis of the EMC-situation of the system is not possible, but parameter examinations can be done. They allow to fix boundary values being of importance for the partitioning and the requirement description of subsystems under EMC-constraints. The setup of the zone model and the looking for relevant intra-system-measures may profit from these studies.

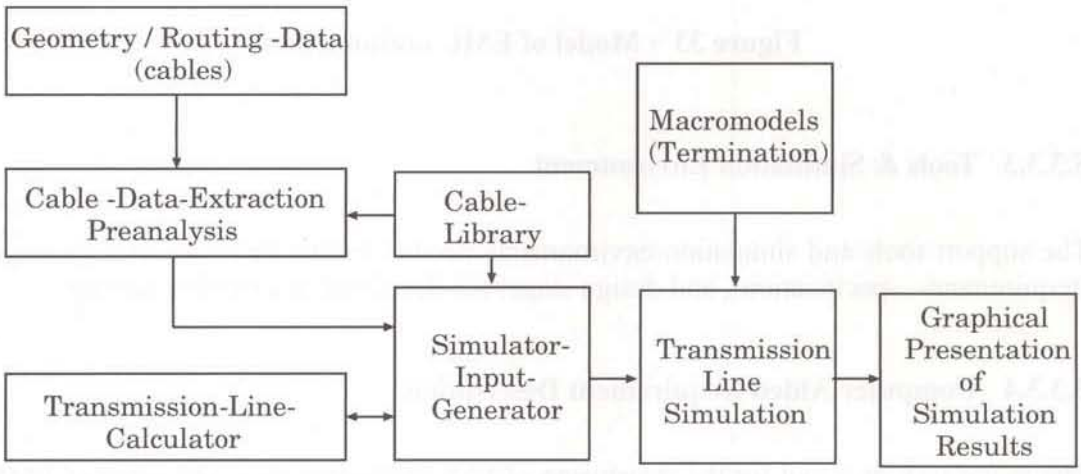

Figure 34 : Simulation tools for transmission line analysis

Figure 34 shows the most important moduls of a simulation tool for Transmission Line Analysis. Beginning with the data supplied by a routing system and a cable library a data processing is necessary. The pure geometrical data are transformed into logical connections by the data extractor. The next step is the calculation of the electrical transmission line parameters 'characteristic impedance' and 'phase velocity'. Here, a TEM wave propagation is assumed. Input files for the simulators can be generated from transmission

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line parameters and the extracted geometrical data. Currently the simulators FREACS, COMORAN and Spice are supported. They need for the simulation of propagation and radiation characteristics models for transmission lines and terminations. These models will be made available by a macromodel library. In order to present the simulation results in a user friendly way, the application of a technical-scientific user interface is planned. It will present the results in cartesian charts, polar and Smith-charts. Aim of the tool is to display the results of the simulation at the design stage as well as the results of the analysis in the validation stage.

5.3.4 Rule Based Advisory System

The simulation of physical effects, which may be of thermal, climatic, mechanical or electromagnetic origin, reaches its limits with rising system complexity because of high computation time, high number of data and huge numerical problems to be solved. Therefore, the design of systems, subsystems (modules), and components has to be supported by rules and application knowledge. This support can be provided by rule based advisory systems which allow a time and cost efficient design and development of systems and subsystems.

In the area of EMC-effects on printed-circuit boards the concept of an EMC-advisory-system has been developed which is introduced in the following. The idea in this concept is to rebuild the general procedure of EMC-experts. Afterwards an overview about the primary stage (transformation) of the EMC-review process is given. The goal of the transformation stage is to reduce the complexity of a given net without changing the original EMC-characteristic. The next paragraph gives an overview on the parameter variation tool **RAFIG**. Using this tool parameter studies can be performed to examine reflection-effects in digital circuits. This allows the development and verification of rules for knowledge-based analysis procedures. At last the results from examinations of reflection-effects in three-point nets are presented. These examinations especially deal with the influence of the net topology on the reflection behaviour and show the great impact between them.

5.3.4.1 EMC-Review Process as basis of an EMC-Advisory-System

Nowadays, the EMC-optimization of PCB-layouts is carried out quite often with various manual operations which need test-boards. Fast changing market conditions require a more systematic approach. The aim is that as many tasks as possible should be done by an advisory-system automatically or partly automatic, instead of specially skilled experts. The EMC-expert should have the possibility to concentrate on those cases that can not be treated automatically. An automatic localisation of the noise problems as well as the explanation of suitable steps for the improvement and their validation are required.

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General Procedure of EMC-Experts

The voltages of single subnets in a layout can be calculated by simulation, appropriately for EMC examinations. A reflection examination especially of complex subnets is very tedious if only simulators are used. An EMC-expert cannot assign calculated interference effects and their noise sources if they exceed a certain complexity. The evaluation of measures for the avoidance or reduction of reflections is only possible if the nets are quite simple and the quantity of nets is limited. Therefore, the expert tries to reduce the subnet complexity by well-known partitioning strategies. The net structure is simplified until the expert recognizes a known structure. During this transformation the main characteristics necessary for the analysis and diagnosis are maintained because appropriate rules and heuristics are selected.

The structures known by the expert form classes of net types. The examined subnet can be mapped on these net types if appropriate net transformations are used. The information about these net types enables the expert to carry out further examinations. The validity of the net transformations carried out before is the basis for the results being also valid for the considered subnet. The two stages "Classification" and "Transformation" can be distinguished.

Classification: Often experts have heuristic knowledge with regard to net classes showing the same behaviour concerning the examined interference. So the procedure is to classify the examined net. If this is done successfully, an analysis of the net after the characteristics of the class is possible. Otherwise, the expert will try to simplify the net.

Transformation: The expert recognizes in a net effect that can be obtained in a more simple way. Often neglectable electrical short transmission lines occur, for example, or a net has more than one receiver, which can be collected to an accumulation group. After each failure of classification the expert decides whether the application of a further transformation method to simplify the net is necessary or not.

The EMC-Review-Process

With the EMC-review a model for the systematic extension of external data as well as the knowledge acquired within the EMC-advisory-system is introduced. The EMC-review process is realized through the EMC-advisory-system and is valid for the examination of interferences on PCBs. Therefore, the following five phases can be distinguished, whereas the rules developed concerning the electromagnetic compatibility are part of every single phase.

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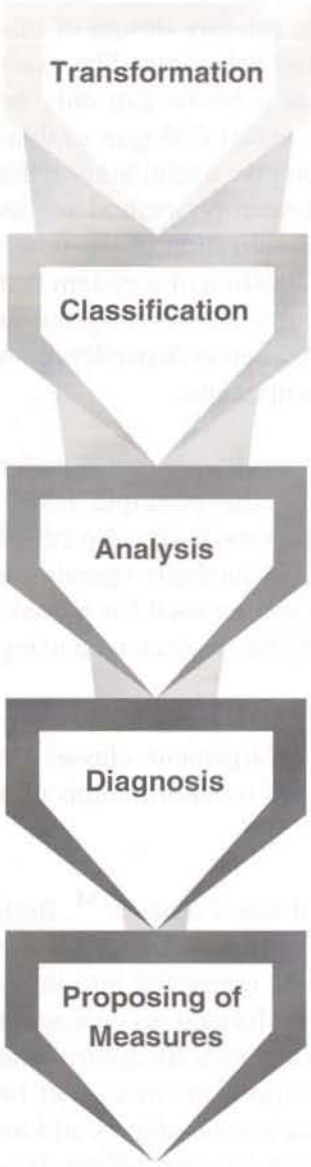

In the review-phase **transformation** the input data are rearranged for further investigations. The transformation reduces the complexity of a net without changing the relevant EMC-behaviour.

The **classification** relates the transformed net to a class of nets appreciable to the observed EMC-behaviour. A class provides data which enable statements concerning the following stages "analysis", "diagnosis", and "proposing of measures".

The **analysis** of a subnet examines whether the respective EMC-interference effects have an impact on the functionality of the subnet or the whole circuit. If a failure occurs the subnet is classified as critical, otherwise as uncritical.

In the **diagnosis** only those subnets are examined which were classified as critical in the analysis phase. The aim is to obtain knowledge about the cause and location of the determined noise effects.

On the basis of the diagnosis phase different measures are selected which should cause a reduction or an avoidance of the determined noise effects. This phase is called **proposing of measures**.

In the phases of the EMC-review process, reflections, crosstalk and other EMC-effects are checked separately. In practice, however, the sum of the noise voltage caused by all occurring EMC-effects should not exceed a given maximum value in a subnet. This value depends on the noise margin of the digital gates used in a PCB design to be investigated. Therefore, it is necessary to account for the noise impact of all occurring EMC-effects in concert. This is possible by specifying an EMC-balance for each signal. The EMC-balance determines for each signal, which portion of the overall noise is allowed for the separate EMC-effects.

5.3.4.2 Realization of the Transformation Phase

A necessary precondition for the realization of the transformation phase in a software tool is the exact analysis of the procedure of EMC-experts. Although single transforma-

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tion steps are modelled by methods able to be parametrized, the primary design of this transformation method can only be a first approach to the desired behaviour. The exact coordination of single methods and the transformation stage as a whole can only be reached by a constant dialogue with EMC-experts. Besides the expert dialogue evaluation tools can be applied at this validation, like simulators that can give useful hints at the analysis concerning relevance and correctness of the used transformation method and its parameterization. The knowledge acquisition necessary for the realization of the transformation phases is not a linear process. But it is aimed at the realization of a system that can be optimized in its behaviour time after time. Hereby, results can be imagined at which the selection of transformation methods or their parametrization in dependence on obvious net attributes can be driven by rule-based knowledge components.

With the transformation tool **TOS** (**T**ransformation **O**f **S**ubnets) a software tool is under development performing the transformations without changing the principle EMC-behaviour. The simplifications are driven by defined transformation methods (also called **TOS**-methods) where at the actual implemented version all **TOS**-methods operate on single net units. The **TOS**-methods being already implemented can be used for a transformation within the reflection examination. **TOS** will completely be implemented using C++.

In order to guarantee a most simple and flexible possibility for enlargement, classes are defined containing all attributes being necessary for the control of transformations of a sub net.

TOS can be started with or without a desktop based on the *X Window System*™. Both versions have in common that the PCB descriptions are read in from a **SULTAN**-file (**S**tandard **U**niversal **L**ayoutinformation **T**ransport l**AN**guage) and converted into internal data structures. After the application of **TOS** -methods the transformed nets are again written in **SULTAN**-format. The desktop offers a variety of possibilities for control and parametrization of single **TOS**-methods. In an object-browser transformations can be started for single nets or a number of nets. Through the duplication of objects and an individual parametrization of all transformation methods defined for each object, it is possible to do several transformations being driven under different aspects. To examine the structure of the original and transformed nets the amount of nets can be presented graphically. In future releases of **TOS** it will be possible to involve arbitrary evaluation tools that supply **SULTAN** as standard interface format. So, **TOS** offers a great number of possibilities for manipulations of nets varying in sequence and parametrization of **TOS**-methods. Moreover, the result of transformations can be validated with different evaluation tools.

5.3.4.3 Rule And Freacs Input Generator (RAFIG)

RAFIG enables the user to examine the reflection behaviour of arbitrary net structures due to single parameters. The aim is to get rules for a correct layout-design, and to scale measures for the improvement of the reflection behaviour. Because of the user-friendly desktop of the parameter editor **cope** it is also possible to generate single input files for

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the simulator **FREACS**. Therefore it is not necessary to have exact knowledge about the simulator input language **TANDEL**.

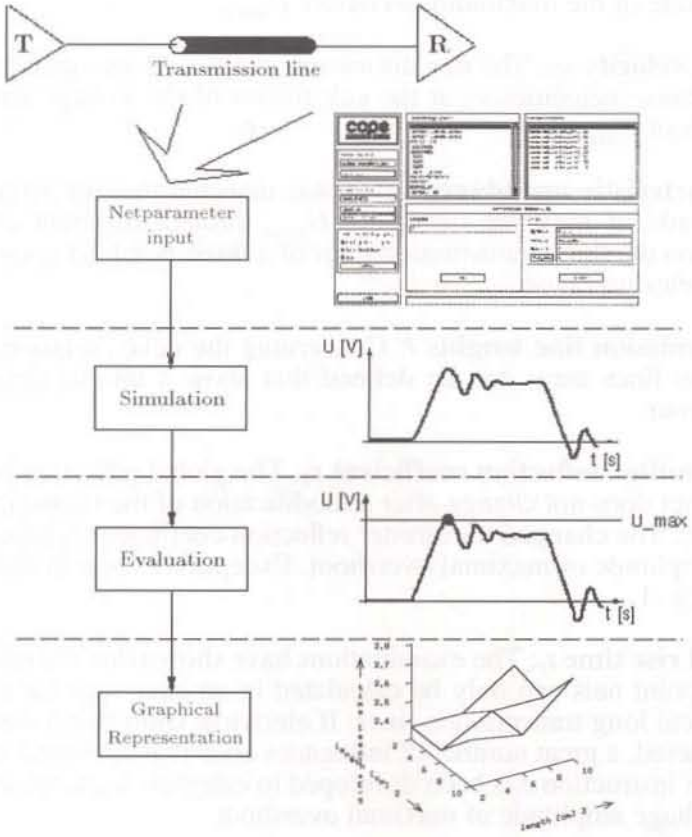

Figure 35 : Concept of RAFIG

The structure of **RAFIG** is presented in Figure 35. In the first step the parameters of a net are defined using the parameter editor **cope**. A parameter range can only be assigned to two of the net parameters at most. For each equidistant support-point of these parameter ranges time dependant voltage flows of the parametrized net are simulated with **FREACS** in the next step. Afterwards **RAFIG** evaluates characteristic values of the simulated voltage flows suitable to judge the reflection behaviour. The result of this evaluation can now be presented with the graphic tool **AnaRes**. Hereby the selected characteristic value of the temporary voltage flows in dependence of the varying parameters are presented.

5.3.4.4 Reflection Behaviour of Three-Point Nets

In this work the reflection behaviour of three-point nets was examined. Transmission lines were examined on which only Quasi-TEM-modes were propagating. The transmission lines were terminated with resisters. Therefore, the effects of all net parameters of a three-point net on the reflection behaviour were analysed.

The net parameters were identified and the ranges to be examined were defined by tech-

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nical relevant data. The examined parameters are:

- **Transmitter source voltage** U_q: A transformation instruction has been developed to consider the influence of the transmitter source voltage U_q on the voltage amplitude of the maximum overshoot U_{max}.

- **Phase velocity** v_p: The transformation instruction was deducted to consider arbitrary phase velocities v_p at the calculation of the voltage amplitude of maximal overshoot U_{max}.

- **Characteristic impedance** Z_L: It was detected that the influence of the voltage amplitude of maximal overshoot U_{max} through different characteristic impedances on the three transmission lines of a three-point net is only small in the technical relevant range.

- **Transmission line lenghts** l: Concerning the delay, relations of the three transmission lines areas can be defined that show a unique characteristic reflection behaviour.

- **Transmitter reflection coefficient** r_s: The global reflection behaviour of a three-point net does not change after a modification of the transmitter reflection coefficient r_s. The changed transmitter reflection coefficient r_s influences only the voltage amplitude of maximal overshoot. Exceptions occur at the special cases $r_s \cong 0$ and $r_s \cong -1$.

- **Signal rise time** t_r: The examinations have shown that the reflection behaviour of three-point nets can only be calculated in an easy way for three-point nets with electrical long transmission lines. If electrical short transmission lines have to be considered, a great number of influences arise that are rather complex. A transformation instruction has been developed to calculate a changed signal rise time into the voltage amplitude of maximal overshoot.

Based on the gained experiences the reflection behaviour of a three-point net can be calculated through algorithmic rules. This approach leads to very complex algorithms when a three-point net contains electrical short transmission lines which means that the application of simulators cannot be avoided. In order to perform a fast analysis procedure without simulators, experiences for the establishment of a knowledge-based model were used that allows the determination of an approximated value for the voltage amplitude of the maximum overshoot in a three-point net. This model was implemented as a function in the programming language C.

With respect to the difficulties that arise at the consideration of the influence of the transmitter transmission line length l and the transmitter reflection coefficient r_s on the voltage amplitude of the maximum overshoot, limitations have to be accepted for the validity area of the model concerning this parameter. The model was verified heuristically with a high number of simulations. The occurring deviations are less than 10%. Further more, a comparison was proceeded between a simulation applying a macromodel as termination and the new knowledge based approach. The results allows an interpretation of the data from the knowledge based approach as an worst-case estimation.

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5.3.5 Generation of Macromodels

Within the activities of macromodel development for complex analog components a tool to generate model structures was developed. The generation of model structures is based on the block-oriented modelling concept described in the following section. Afterwards the tool MASE (MAcromodelling Synthesis Environment) for the generation of model structures will be introduced.

5.3.5.1 Block-oriented Modelling Concept

At the beginning of the block-orientated modelling analog components are structured into pre-defined classes concerning their characteristics and their functional behaviour. The components of one class are examined with regard to their input-, output- and transfer-behaviour, and the results of these examinations are to be compared to each other. Special blocks are defined for common as well as for different characteristics to be modelled.

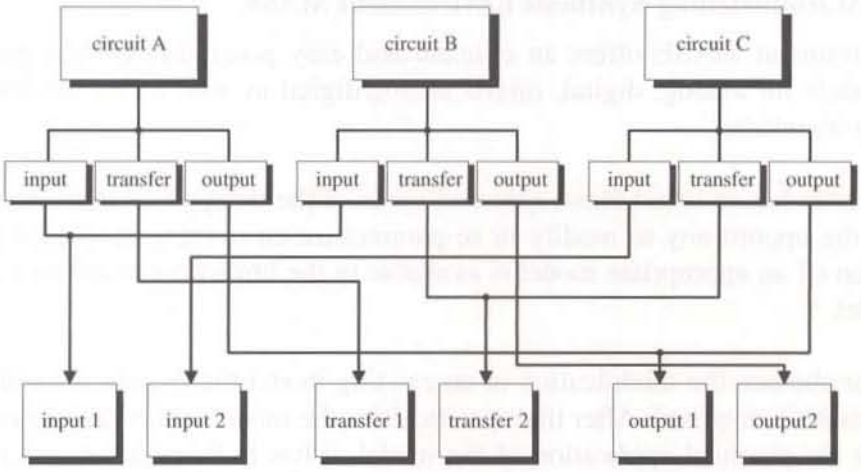

Figure 36 : Example of the block definition

Figure 36 presents an example of the block definition. The components of a particular class - here called A, B and C - are analysed and compared with each other. Such an analysis may suggest that the input behaviour of component A quite closely matches that of component B. As a result only one input model is developed for A and B that describes this characteristic within the required accuracy. As the input behaviour of part C is different from both A and B a separate block has to be defined. The same procedure is applied for other characteristics like transfer or output, for example.

In order to determine matching characteristics of circuits, their behaviour is examined in much more detail than given in the example. The input-behaviour for instance is refined to a more detailed description which leads to a higher chance to find matching characteristics. The blocks are defined in such a way that they can be used for the representation

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of simple components as well as component-internal functional units.

An advantage of higher granularity of the behavioural characterisation is the better adaption of a macromodel that is composed of interconnected blocks in different design phases. It is very difficult to define an optimal refinement of blocks because this task highly depends on the circuit in question and its properties.

The application of a block-oriented modelling methodology reduces development time and costs significantly, because new models have not to be designed from scratch but can be assembled from existing and tested parts. New designs have to be considered only for the peculiarities of a circuit that are not covered by existing blocks. Furthermore the definition of blocks by specification offers the perspective of model generation by an automated connection of blocks.

The concept of block-oriented model development of analog components is the basis for the tool MASE being developed for automatized model generation.

5.3.5.2 Maromodelling Synthesis Environment MASE

The environment MASE offers an efficient and easy possibility for the generation of macromodels for analog, digital, mixed analog/digital as well as for electric and non-electric components.

First, the user has to select class, type and name of the component to be modelled. The user has the opportunity to modify or re-parametrize an existing model for the desired application (if an appropriate model is available in the library) or to create a completely new model.

If the user chooses the modification of an existing model the specification of the model characteristics is required. After this specification, the model will be generated automatically. For the practical application of the model, it has to be parametrized in a further step. The result of the whole process is a ready to use model description, which fulfills the model specification.

In case of parametrizing an existing model, the user has to specify the corresponding circuit parameters. Based on this an available model will be parametrized by transforming the circuit parameters into the correspondent model parameters automatically.

The generation and parametrization of a model structure is done by the application of the several components of MASE as shown in Figure 37.

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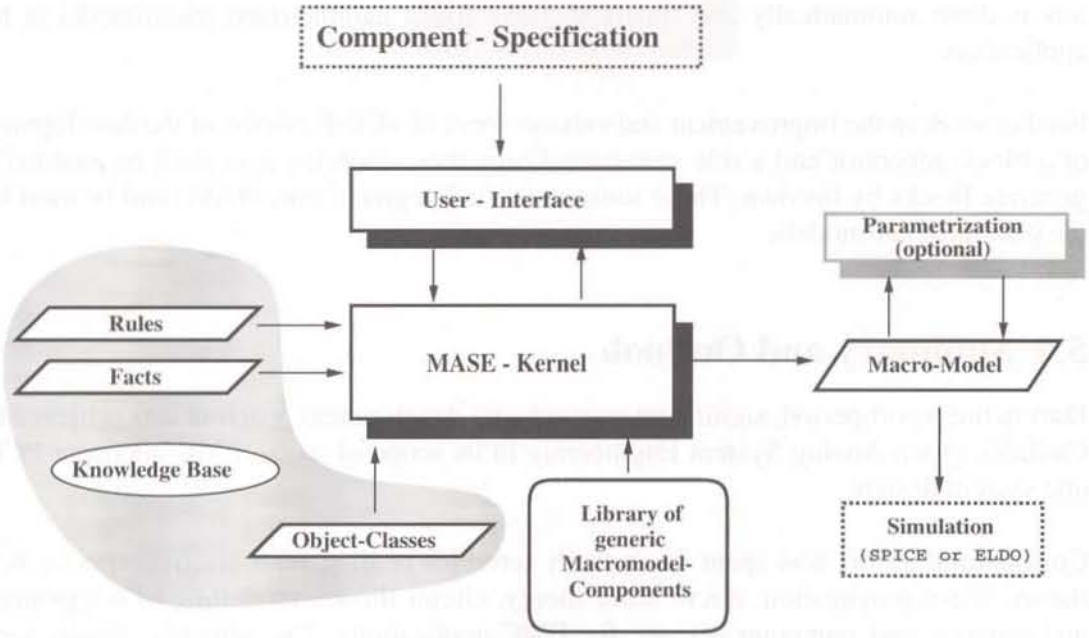

Figure 37 : Internal structure of MASE

MASE-Kernel: The MASE Kernel consists of the tool CLIPS which was developed by the NASA [NASA 1991/1992; "CLIPS 5.1 Reference Manual"; Software Technology Branch; Johnson Space Center; NASA; Houston; TX, USA]. CLIPS is used for the processing of expert knowledge in form of rules. The rules are described in a special syntax. CLIPS follows all the rules along the user specification and generates the macromodel from the single blocks. At the same time an examination of consistency is done which shows missing inputs and eliminates false ones.

Knowledge Base: To generate models a respective knowledge about modelling is necessary. This expert know-how is filed in form of rules and facts. The knowledge describes the characteristics of the model blocks and determines the conditions for connecting different blocks to a macromodel.

Library: The library contains different model blocks that are needed for model generation as well as complete macromodels which can be adjusted with MASE regarding the desired specification.

Parametrization: The model generation is finished by the specification of component parameters and the conversion of these data into model parameters. As in most cases the component parameters are not equal to the model parameters a transformation has to be done with respect to given computation rules. Therefore, the model parameters are described in the language SYBES. The specification of the component parameters is done via the editor COPE. After the specification the computation of the model parame-

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ters is done automatically and finally the user has a parametrized macromodel at his application.

Further work in the improvement and enhancement of MASE consist of the development of a block-generator and a rule-generator. Using these tools the user shall be enabled to generate blocks by his own. These tools could be integrated into MASE and be used for the generation of models.

5.4 Summary and Outlook

During the report period, significant research and development progress was achieved by Cadlab's group Analog System Engineering in its scope of work 'EMC-adequate PCB- and system design'.

Considerable effort was spent in research activities dealing with electromagnetic field theory, wave propagation, micro wave theory, circuit theory, modelling of components and circuits, and computer science for EMC-applications. The scientific results were documented by a large number of scientific publications and three PhD theses which were completed during the report period:

- D. Theune: "Robuste und effiiziente Methoden zur Lösung von Wegproblemen", April 1994,
- T. Maeser: "Berechnung des Übertragungsverhaltens von Leistungsstrukturen integrierter Schaltungen", December 1994,
- Stefan Öing: "Elektromagnetisches Strahlungsfeld elektronischer Komponenten und Systeme", December 1994.

Furthermore, the EMC-Workbench, a software package for supporting the EMC-adequate PCB-design, was further developed. The software was used within a large number of industrial application projects for the support of an EMC-adequate design of high-speed printed circuit boards within the development departments of Cadlab's industrial partner SNI. The experience gained during these projects was consequently exploited and the EMC-Workbench obtained product maturity. In order to evaluate the market for EMC-tools and to publish Cadlab's results, it was presented at various scientific conferences as well as at commercial exhibitions and fairs. The industrial and commercial exploitation of the software could be realized by its transfer to the new EDA-company INCASES Engineering GmbH founded in November 1994. With the software also the major part of the EMC-Workbench development team moved to INCASES in order to guarantee the necessary know-how transfer, the further development of the software, and its maintenance.

As a consequent further development of its recent activities, the global objective of the Analog System Engineering group is the development of tools and methodologies for the design-support of entire systems with regard to EMC-constraints, which also means that the physical realization of the system to be developed will be taken into account. The

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aim is the development of a System-Workbench which supports the system designer. For this purpose a generalized design process was defined which allows the integration of a process for the optimization of the EMC-behaviour of the entire system. During the report period the available experience and knowledge, gained during the development of the EMC-Workbench, was transferred to this large problem area and basic research and development activities were started in order to prepare the corresponding restructuring and new adjustment of the Analog System Engineering group.

The research activities were supported significantly by nationally funded projects in the Joint European Submicron Silicon Programme (JESSI AC-5, JESSI AC-12) and the Microsystem Technology initiative of the German Government, Department of Research and Technology.

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6 Technical Management Group and Computing Centre

6.1 Baseline

The mission of Cadlab's "Technical Management Group, TMG" and the "Computing Centre CC" is to offer general services to all Cadlab teams.

Main objective of the TMG Group has been the provision of support for consolidating Cadlab's efforts in the area of "Computer-Aided Concurrent Engineering, CACE", while the Computing Centre is responsible for Cadlab's computing infrastructure.

From a technical point of view central focus of attention has been the evaluation and preparation of scientific material, the establishment and maintenance of external contacts as well as the internal coordination of Cadlab's R&D processes. Driving force of all these activities has been the request for creating an appropriate environment for the further introduction and implementation of Cadlab's leading theme CACE in its administrative and technical aspects according to the pre-supposed planning horizon (about three to five years, starting in 1993).

Another central topic have been measures for assuring that Cadlab's software development projects and their envisaged results satisfy the required quality criteria in order to facilitate the transfer of Cadlab's R&D work into potential SNI products. The framework for these quality criteria is given by SNI's quality principles, expressed in the SNI Process Handbook for Application Software, its Cadlab specific supplements and the ISO standard for quality assurance systems.

In addition, TMG had to deal with

- internal and external promotion and presentation of Cadlab and of its results;
- support and consultancy for the acquisition and management of national and international, collaborative projects;
- analysis of the CACE problem space in practice (CACE requirements engineering).

All these technical TMG activities have been complemented by a number of administrative coordination efforts, which included budget-controlling and commercial support of running and new Cadlab projects, and processing of all contractual issues. Finally, TMG has acted as interface to relevant departments within SNI and Paderborn University, especially for the organisation and realisation of the (forthcoming) move of Cadlab to its new premises.

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6.2 Work During the Report Period

6.2.1 CACE Requirements Engineering

In continuation of efforts started in 1993, work in 1994 concentrated on the participation in the CAI-project of SNI's plant for midrange computer systems. "CAI" stands for "Computer Aided Industries" and denotes "large restructuring and business re-engineering approach set-up to enhance the competitiveness of SNI's midrange operations. Within the global CAI-restructuring effort of this plant, Cadlab's task was to design a conceptual schema for component part data and to develop an import/export interface for parts library data. Examples for components are integrated circuits, capacitors, printed circuit boards, screws, or cases. A conceptual schema describes information types associated with these components, like size, weight, unique identification number, supplier, programming information, etc. A strong motivation for Cadlab to participate in this project was to understand current data handling practice and especially what kind of problems have to be solved by future software solutions.

Results of Cadlab's participation in the CAI project have been presented and published in various contexts, among others within JCF Subproject 4 "Evaluation

A Data Schema for Parts Data

During the report period a sub-project of the CAI-project was finished which was started in April '93. The goal of this sub-project was to define a data schema for technical parts data. This schema should serve as a basis for system integration and migration.

After an extensive research and analysis phase of the existing parts data used within the UNIX computer manufacturing plant, the project team defined a gross schema for technical parts data. The schema supported a top-down approach, so that on the top level only "large" data entities (like libraries) are visible, and details are left to lower levels. Also, in contrast to schemes like EDIF, a more pragmatic approach was followed: data containers like libraries were explicitly modelled, because for administration purposes these entities are very important. The CASE Tool "Innovator" was used to document the schema.

The main problem with data schemes of such a global scope is to supply the appropriate level of detail. If the schema shows too much detail, it has to be updated and maintained by a lot of people in parallel in order to be useful (i.e., correct and up-to-date). Effectively, this means that the schema has to serve as a "master" for all parts databases within the factory. On the other hand, if the schema shows too little detail, only trivial entities and relations are captured, so that very few people (like novice users) can profit from studying it. The most useful approach would be to have a hierarchical schema as database master, capable of driving heterogeneous databases and suitable for local maintenance by database administrators.

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An Import/Export Interface for Parts Library Data of the EMC-Workbench

When operating the EMC Workbench (of chapter 5.3), employed by the UNIX computer manufacturing plant for assessing the EMC properties of PCBs data about electronic parts have to be utilized. For each pin of an electronic device (like an IC) a simulation model is necessary in order to calculate signal transmission effects on connecting wires. The relation between a given simulation model and a certain pin is specified within the Parts Library of the EMC Workbench. E.g., many pins refer to the same simulation model, because their electrical characteristics with respect to EMC effects are equivalent.

Within most companies data about parts is stored and maintained by a component information management system (CIMS). In order to utilize this data for the EMC Workbench, an import/export interface has been implemented to enable the exchange of data in and out of the EMC Parts Library in a neutral format during a follow-up sub-project of the above mentioned one. The format defines two ASCII tables, one for parts data and one for pin data. This format was designed in such a manner that an immediate processing by a PC-based database is possible.

Furthermore, a second version of this import/export interface has been implemented on top of an object-oriented database BISOM, taken from Cadlab's DBF project. For this experiment, the file-system-based Parts Library of the EMC Workbench was substituted by BISOM's OODB technology. The Library was filled with test data in order to compare both solutions (BISOM- vs. file-system-based).

6.2.2 Software Engineering and Quality Assurance

One of the goals of the Technical Management Group was to ensure that Cadlab software development projects meet industrial quality standards. Therefore in 1994 continuous effort was spent to adopt the guidelines of the SNI Process Engineering Handbook in the ongoing software development projects in all Cadlab working groups. Care had to be taken to apply those guidelines in a manner adequate for the special requirements of Cadlab with its deep integration of research and development. The necessary adaptations are documented in the "Cadlab Handbook for Software Development Projects"; a completely revised issue of this handbook has been finished and introduced in 1994.

Support of five Cadlab projects was continued during 1994: "EMC Workbench", "Advanced Editing Systems", "Intelligent Framework Services", "Database Federation Services", and "STEP/EXPRESS Environment EXPREME".

A member of TMG played the role of the "technical controller" in those development projects. According to the SNI Process Engineering Handbook the technical controller checks at milestones whether a project proceeds according to the pre-defined development process and that the required results are achieved. Furthermore, the technical controller supports the project members by consultancy on topics concerning software engineering, project management or quality assurance on demand. Another member of

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TMG participated actively in the successful T50 test for EXPREME 1.0.

Furthermore, in 1994 communication links with the technical controller of SNI AP in Paderborn were established in the context of quality management according to ISO 9001. As part of SNI AP, Cadlab achieved the DQS certificate for an ISO 9001 compliant quality management system in March 1994 with regard to its software development activities.

6.2.3 Promotion and Presentation

Besides presenting Cadlab at various opportunities TMG contributed to a number of external brochures and newsletters (e.g., to the Newsletter of the IEEE Technical Segment Committee on "Engineering of Complex Computer Systems") with references to Cadlab.

Internally, TMG coordinated

- the production of Cadlab Annual Report '93;
- the Cadlab contribution to the "Who-is-Who" brochure of Paderborn University;
- the development of a Cadlab "Corporate Identity" concept;
- the production of a proposal for improving Cadlab's software development environment;
- Cadlab standard slides sets.

In addition, TMG contributed to the analysis of Cadlab's documentation environment and produced a number of templates and forms for documentation and promotion/presentation purposes, e.g., for slides and project documentation. TMG participated in establishing a Cadlab World-Wide-Web home page and in filling it with contents.

TMG members participated in various publication efforts, e.g., in Cadlab Reports 01/94, 09/94, 11/94, 13/94, 14/95 and 15/95.

6.2.4 Project Acquisition and Coordination

During the report period TMG contributed to early initialise proposal production efforts in the context of the first call for proposals (issued on December 15) of the EU Forth Framework Programme for the following areas:

- knowledge asset management and data base federation (in cooperation with group IT);
- electromagnetic compatibility and interconnect design support tools and interfaces (in cooperation with group ASE);

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- process modelling/process technology, multi-media assisted distributed tele-engineering and framework-based support for distributed engineering (in cooperation with SNI BU ES CE);
- hardware/software co-design/co-verification (in cooperation with the Cadlab group IT and SNI SU MR PD).

TMG had coordinated ASSET Task D3 "Framework Components", which included the task's day-to-day management (progress and effort reporting, milestones tracing, etc.) and the organisation of D3 meetings and workshops. In addition, preparation and (successful) participation in the ASSET technical and managerial reviews represented considerable efforts of TMG.

Administrative and technical consultancy has been given to SNI SU AP 44 in the context of the ITHACA project and to the Cadlab project group dealing with the SYDIS project. The Cadlab group ASE was supported in managing the projects AC-5, AC-12 and Mst-Bib from an administrative point of view. In conjunction with the JCF Project Office the organisation of Cadlab resources in the JCF project has been coordinated. At the beginning of the report period, Cadlab TMG finished its consultancy efforts in the ADVANCE project and passed its management responsibility to the ADVANCE project management team (including SNI BU ES CE).

6.2.5 Computing Centre

The main task of the group of the Computing Centre is the support and maintenance of an efficient programming environment for all Cadlab employees. This particularly includes the assistance of the employees and student assistants, the acquisition and installation of additional hardware and software tools, the improvement of the existing network and the task to keep all systems operational.
Furthermore the Computing Centre support the Cadlab external framework group which spun off from Cadlab in a product transfer process in 1992. These employees have their offices in the same building and use the same programming environment as all Cadlab employees.

Acquisition of Systems and Modules

The existing hardware equipment, mainly Sun and Silicon Graphics workstations, was expanded with additional workstations and Personal Computers. In order to supply a sufficient number of workstations and computing power for the growing number of employees and student assistants some workstations were acquired and other workstations were expanded with local disk capacity and memory. Old servers (SNI Targon/35) were replaced by two new Sun workstations. In addition a high end parallel computing server (SGI-Power Challenge) was installed.
The hard- and software for data backups was updated and expanded and printers were equipped with Ethernet Network interfaces.

6.2.5.1 Networking

Via a workstation configured as a gateway, the local area network at Cadlab is part of the

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network of Paderborn University. Besides the overloaded existing permanent link a semi-permanent ISDN link to Paderborn University was established. Due to the links it is possible to exchange electronic mail and data directly and to work interactively on computers at the university with acceptable performance. It offers also the entry to other networks worldwide

To improve the performance of Cadlab's local area network a multiport Ethernet bridge was installed. The bridge allows for a fragmentation of the network into four parts using the existing cabling. Four more ports were used to connect servers directly to the bridge and the Ethernet backbone was replaced by the internal 175Mbit/s bus of the bridge.

In addition to the existing standard network services a World Wide Web server was installed to offer information of Cadlab's activities to the public and to improve the availability of internal informational sources.

Operating System Software and Tools

One of the main tasks of the Computing Centre group is to build up and preserve a homogeneous programming environment which, at best, is available on all different hardware respectively operating systems platforms.

With the support of some employees representing the other project groups at Cadlab the installation of locally used tools like TeX, FrameMaker, printer spooler, gnu tools etc. was improved.

Some more Sun workstations were installed with the operating system Solaris2. As the new version Solaris2.4 turns out to be stable and comes up with sufficient performance, in contrast to the older versions, a general change to Solaris2 is planned.

6.2.6 Parallel Computing

In fall 1994 a small project group named "Parallel Computing" was formed to concentrate and coordinate Cadlab's activities in this field. The first proposition was to evaluate software tools for load balancing and parallel programming on workstation clusters as well as parallel computer hardware. These tasks are ongoing.

In addition, work was set up towards an automatic generation of code from system specifications based on extended Petri Nets, a specification model that is used within the group PSM. This work started with a definition of a textual language for net representations on which the generator will operate.

6.3 Summary and Outlook

One of the major achievements of TMG during the report period has been the acceptance by all Cadlab groups as central information switchboard and competent support centre for all kind of problems. This has represented a quite difficult but also challenging effort for TMG due to the mutually orthogonal responsibilities of its members.

Together with the Computing Centre a number of successful endeavours jointly per-

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formed with other Cadlab teams and SNI BU ES CE contributed to the fact, that TMG has been recognised as a well-accepted organisation both within Cadlab and externally:

- industrialisation of the STEP/EXPRESS Environment EXPREME: software engineering and quality assurance consultancy of TMG contributed to keep the T50 deadline of this project as planned;
- acquisition and coordination of projects; including ITHACA, ASSET and ADVANCE
- administration of all contractual Cadlab issues
- successful finalization of the CAI schema sub-project with the SNI plant for mid-range computer systems;
- publishing and presenting the results of Cadlab's work;
- extending and maintaining a complex networked computing environment for more than 200 internal and external engineers and scientists;

Due to major Cadlab internal restructuring (merge of SET and BT groups to IT group) and the personal involvement of TMG members in this and in related (IT) projects, it has been decided to transfer the technical TMG tasks and persons to the Cadlab project groups by the 3rd quarter of 1994. Administration and Computing Support together with parallel Computing have been kept as centrally organized activities.
A major task anticipated in 1995 is the move to Cadlab's new offices in the former Nixdorf headquarters at Paderborn, Fürstenallee. This will involve a complete renewal of Cadlab's technical infrastructure and computing network.

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III Publications, Funded Projects and Scientific Collaborations

7 Publications and Major Documents

7.1 Cadlab Reports

- "Eine kurze Einführung in Concurrent Engineering", J. Stauß (Cadlab Report 01/94)
- "Federation and Stepwise Reduction of Database Systems", E. Radeke, M. H. Scholl (Cadlab Report 02/94)
- "Object Migration in Federated Database Systems", E. Radeke, M. H. Scholl (Cadlab Report 03/94)
- "Zur Entwicklung von Mikrosystemen unter EMV Gesichtspunkten", W. John, J. Schrage, M. Gutzmann (Cadlab Report 04/94)
- "Parallel Validation of STEP Files", G. Lehrenfeld, W. Müller, N. Wiechers (Cadlab Report 05/94)
- "Implementing Simultaneous Design: A Case Study", D. Nyhuis, W. Müller, K. Gröning, F. Buijs (Cadlab Report 06/94)
- "Defining the Relational Grammar of PJ - A Case Study", G. Lehrenfeld, W. Müller (Cadlab Report 07/94)
- "Management of Concurrent Design Processes", J. Tacken, E. Kleinjohann (Cadlab Report 08/94)
- "On the Need to Address Non-Functional Aspects in Concurrent Engineering", J. Dunkel, K. Ryan, F.-J. Stewing (Cadlab Report 09/94)
- "A Design Model for Concurrent Engineering of Heterogeneous Systems", M. Brielmann, B. Kleinjohann (Cadlab Report 10/94)
- "Computer Aided Concurrent Engineering (CACE) System Requirements", J. Strauß (Cadlab Report 11/94)
- "Controlling Cooperation and Recovery in Nested Transactions", A. Meckenstock, R. Unland, D. Zimmer (Cadlab Report 12/94)
- "Requirements for ECBS Environments: A Case Study", F.-J. Stewing, J. Strauß (Cadlab Report 13/94)
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- "Das SIR-Datenschema", J. Becker, F. Buijs (Cadlab Report 34/94)
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- "Ein Konzept für kooperierende Transaktionen in Entwurfsumgebungen", A. Meckenstock, R. Unland, D. Zimmer (Cadlab Report 37/94)
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- J. Schrage: "Konzept eines Testsystems zur Durchführung von EMV Validierungen beim Entwurf komplexer signalverarbeitender Mikrosystemkomponenten", Tagungsband zum 1. Workshop 'Methoden- und Werkzeugentwicklung für den Mikrosystementwurf', Karlsruhe (Germany), 15. November 1994, pp. 199-206

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- J. Tacken, L. Kleinjohann: "Management of Concurrent Design Processes", CEEDA, Bournemouth, April 1994, pp. 43-48

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- D. Wagenblaßt, J. Müller, W. John, E. Griese: "An Approach of Rule Development for Reflection and Crosstalk Effects on Printed Circuit Boards", Proceedings of the 12th International Wroclaw Symposium and Exhibition on EMC, Wroclaw (Poland), 28. June - 1. July 1994, pp. 17-21

- D. Wagenblaßt, W. Rissiek: "Layoutanalyse analoger Schaltungen basierend auf einem erweiterten Bibliothekskonzept", Tagungsband zur 3. GME/ITG Diskussionssitzung 'Entwicklung von Analogschaltungen mit CAE-Methoden', Bremen (Germany), 29. - 30. September 1994, pp. 151-156

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7.4 PhD Theses

The following PhD Theses have been completed during the report period:

- H.-J. Kaufmann: "Eine objektorientierte Software-Architektur für graphische Editoren", January 1994
- F. Buijs: "Automating the Logic Synthesis of Arithmetic-Logic-Units", January 1994
- B. Kleinjohann: "Synthese von zeitinvarianten Hardware-Modulen", February 1994
- L. Kleinjohann: "Integrierte Entwurfsberatung auf der Basis erweiterter Prädikat-Transitionsnetze", April 1994
- D. Theune: "Robuste und effiiziente Methoden zur Lösung von Wegproblemen", April 1994
- T. Maeser: "Berechnung des Übertragungsverhaltens von Leistungsstrukturen integrierter Schaltungen", December 1994
- Stefan Öing: "Elektromagnetisches Strahlungsfeld elektronischer Komponenten und Systeme", December 1994

7.5 Master Theses

The following master theses have been completed at Paderborn University under the responsibility of Cadlab:

- M. Becker: "Entwurf und Realisierung objekt-orientierter Basiskonzepte zur anwendungsbezogenen Datenintegration auf der Grundlage eines objekt-orientierten Datenbanksystems"
- A. Eickermann: "Entwurf und Realisierung graphischer Konzepte für die anwendungsbezogene Repräsentation von Objektgraphen in einer Integrationsumgebung."
- H. Hähnel, M. Wehmeier: "Entwicklung von Regeln für ein Beratungssystem zur Unterstützung des EMV-gerechten Leiterplattenentwurfs"
- A. Hänsel: "Erstellung eines Konzeptes von Klassifikationsmerkmalen unter EMV-Gesichtspunkten zur Entwicklung einer Kabelbibliothek"
- M. Heinrichs: "Software-Architekturmodelle von Benutzungsschnittstellen"
- T. Hesse: "Automatische Wissensakquisition und Konstruktion von Klassifikationen anhand konzeptueller induktiver Lernverfahren"
- H. Nait-Challal: "Berechnung der charakteristischen Parameter von Leiterplattenverdrahtungen in Multilayertechnik durch Lösung eines gemischten Randwertproblems"
- M. Sajady: "Dielektrische Körper im elektromagnetischen Feld"

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- S. Sekander Sajady: "Stromverteilung auf elementaren linearen Antennen in Gegenwart von Beugungskörpern"
- H. Schmidt: "Lagenzuweisung und Netzordnung für die globale Verdrahtung beim EMV-gerechten Leiterplattenentwurf"

7.6 External Talks, Lectures, Tutorials, Panels

- Frank Buijs: "Datenpfadgenerierung: Logiksynthese, Kodierung, Layoutgenerierung", Presentation at OMSI Workshop, Berlin, December 1994
- P. Drescher: "Integration of KAM and CACE - Intelligent Framework Services IFS", ERIKA Meeting, Paderborn, March 1994
- P. Drescher: Demo : "IFS Application ISDS (Intelligent System Design Support", JCF-SP1 Workshop, Karlsruhe, April 1994
- P. Drescher: "Process and System Modelling in Cadlab", Presentation at Dassault, Paris, September 1994
- D. Frei: "An Approach considering EMC-aspects during System Planning", EUROEM 94 International Symposium, Bordeaux (France), 30. May - 3. June 1994
- E. Griese: "EMC-adequate System and PCB Design", EMC Information Day, Brussels, April 1994
- E. Griese: "Anwendung der Leitungstheorie zur Behandlung der vektoriellen Beugung elektromagnetischer Wellen an dielektrischen Gittern", Kleinheubacher Tagung 1994, Schloß Kleinheubach/Main, 10.-14. October 1994
- W. Heijenga: "Vom Schema zur Sicht: Änderungsmöglichkeiten bei der Sichtableitung in einem objektorientierten Datenbanksystem", GI Workshop Grundlagen von Datenbanken, Bad Helmstedt, September 1994
- M. Holeña: "Uncertainty Processing", Poster at JCF-SP1 Workshop, Karlsruhe, April 1994
- R. Kruschinski: "The Hybrid Knowledge Description Language HyKL", Poster at JCF-SP1 Workshop, Karlsruhe, April 1994
- R. Kruschinski: "The Knowledge Evaluation Component (KEC)", JCF SP1 Meeting, Bonn, September 1994
- E. Löschner: "Werkzeugintegration/ Integrierte Entwurfsführung", Presentation at SYDIS Workshop, Bonn, January 1994
- J. Müller: "ROSAR - Rule Oriented System for Analysis of Refelction Effects on Printed Circuit Boards", 1994 International Symposium on Electromagnetic Compatibility, Sendai (Japan), 16. - 20. May 1994
- J. Müller: "Development of Rules for Printed Circuit Board Design under EMC Constraints", 1994 International Symposium on Electromagnetic Compatibility, Sendai (Japan), 16. - 20. May 1994

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- D. Nolte: "Enhancing the Data Openess of Frameworks by Database Federation Services", Presentation at IFIP WG 10.2 Working Conference on Electronic Design Automation Frameworks (EDAF '94), Gramado, Brazil, November 1994
- B. Planken: "Konzept und Prototyp einer Entwicklungsumgebung für die Mikrosystemtechnik", 1. Workshop 'Methoden- und Werkzeugentwicklung für den Mikrosystementwurf' Karlsruhe (Germany), 15. November 1994
- F. Sabath: "Computation of Common Mode Radiation due to Asymmetric Coupling on Printed Circuit Boards", 12th International Wroclaw Symposium and Exhibition on EMC, Wroclaw (Poland), 28. June - 1. July 1994
- H. Schmidt: "Prozeßmodell zur Integration der EMV in die Entwicklung von Mikrosystemen", 1. Workshop 'Methoden- und Werkzeugentwicklung für den Mikrosystementwurf' Karlsruhe (Germany), 15. November 1994
- J. Tacken: "Entwurfssteuerung und -überwachung mit Hilfe von Prädikat/Transitions-Netzen", Presentation at SYDIS Workshop, Bonn, January 1994
- J. Tacken: "Werkzeugintegration/ Integrierte Entwurfsführung", Presentation at SYDIS Workshop, Dresden, October 1994
- D. Wagenblaßt: "An Approach of Rule Development for Reflection and Crosstalk Effects on Printed Circuit Boards", 12th International Wroclaw Symposium and Exhibition on EMC, Wroclaw (Poland), 28. June - 1. July 1994

7.7 Exhibitions

Cadlab results have been presented at the following exhibitions:

- 4. Internationale Fachmesse und Kongress für EMV, Karlsruhe (Germany), February 1994
- EDAC '94, Paris (France), Febr./March 1994
- CAD '94, Paderborn (Germany), March 1994
- CeBIT '94, Hannover (Germany), March 1994
- "First International Workshop on Action Semantics", Edingburgh (GB), April 94
- EMC Information Day, Brussels (Belgium), April 1994
- "2nd International Conference on Concurrent Engineering & Electronic Design Automation (CEEDA '94)", Poole (UK), April 94
- 21st Design Automation Conference and Exhibition, San Diego, (USA), June 1994
- "1994 ASME Computers in Engineering Conference", Minneapolis, MI (USA), September 94

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- EURO-DAC '94/EURO-VHDL '94, Grenoble (France), September 94
- 4th Annual EXPRESS User Group International Conference, Greenville SC (USA), October 1994
- ISATA, Aachen (Germany), November 1994

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8 Funded Projects

8.1 Nationally Funded Projects

During the report period, Cadlab participated in a number of cooperation projects supported by the BMBF or AiF[1] as indicated in Table 1.

Title	Support program	Run time	Project partners
MST-BIB	BMBF (formerly BMFT)	04.91 - 04.95	ABB CEAG LuS, Uni Paderborn, Uni Bremen, Bosch, DOSIS, FH Wiesbaden, FhG-AIS, Hahn Meitner Institut, Krone, Rhode & Schwarz, SRM-CAE, TU Braunschweig, Uni Dortmund, Texas Instruments, Mikron
METEOR	BMBF (formerly BMFT)	07.92 - 12.96	KfK/IDT, FhG-IIs, GMD, MBB, Uni-GH Wuppertal, Siemens, FhG-IIS-EAS, SNI, BOTEC, ebm, ETA, Harting, Jenoptik, Kuhnke, Mannesmann Tally, MicroParts, PROFI Engineering, AST, VDO, TU Berlin, Bosch, TU Chemnitz, Uni Erlangen, Uni Paderborn
MST-UEM	BMBF (formerly BMFT)	06.92 - 12.94	KfK/IDT, FhG-IMT, UniBW München, GMD, Uni Erlangen, TH Ilmenau, TU Magdeburg, FH Augsburg, TU Chemnitz, TU Berlin, Uni Jena
JESSI AC-5	BMBF (formerly BMFT)	07.92 - 06.95	ABB, Bull, DASA, GFAI, ITALTEL, MATRA, Mercedes-Benz AG, Philips, RFT-SEL, THESYS, TU Ilmenau, Vectorfields, Philips Research Labs (UK)

Table 1: Nationally Funded Projects

1. Arbeitsgemeinschaft industrieller Forschungsvereinigungen e. V.

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Title	Support program	Run time	Project partners
JESSI AC-12	BMBF (formerly BMFT)	01.92 - 12.94	ANACAD, Bosch, CSEM, EZM, FhG/EAS, MATRA, Philips, Siemens, SGS-Thompson, S3, TEMIC
OMSI	BMBF (formerly BMFT)	08.91 - 12.94	Humboldt-Universität Berlin, TU Ilmenau, Uni Paderborn
OPAL	AiF	12.92 - 05.95	GFAI, Parsytec
QUELLE	DtA	09.93 - 03.96	GFAI, Widis, Uni Paderborn, TU Danzig
SYDIS	BMBF (formerly BMFT)	01.93 - 12.95	GMD, Uni Paderborn, FhG-EAS, FZI Karlsruhe, SNI
Schnittstellen-synthese	DFG	09.94 - 08.95	numerous partners from several german universities

Table 1: Nationally Funded Projects

8.2 European Funded Projects

In the report period Cadlab participated in the CEU funded projects (ESPRIT) as outlined by Table 2.

Title	Support program	Run time	Project partners
ESIP	ESRIT-II/III	10.93 - 09.95	Bull, ICL, SNI, Siemens, Thompson-CSF, Racal-Redac, Philips (Uni Paderborn assoc. to SNI)
JESSI-Common-Frame	ESPRIT-II	05.93 - 04.95	SNI, ICL, SGS-Th., Siemens, Philips, Racal-Redac, TU-Delft (Uni Paderborn assoc. to SNI)
ASSET I	ESPRIT-III	03.93 - 04.94	Bull, Olivetti, Philips, CAP Debis SSP, Emeraude, TCD, Uni Siegen, SSE, Sysdeco

Table 2: European Funded Projects

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8.3 Reports on Funded Projects

MST-BIB Reports:

- "SNI - Abschlußbericht", September 1994
- "4. Zwischenbericht (Period 01/94 - 12/94)", December 1994

METEOR Reports:

- "Zwischenbericht TP2 - AP2.4 - AT2.4.2 (Period 01/94 - 06/94)", June 1994
- "Zwischenbericht TP2 - AP2.4 - AT2.4.2 (Period 07/94 - 12/94)", December 1994
- "Technischer Bericht (Period 01/94 - 09/94)", September 1994

MST-UEM Reports:

- "Zwischenbericht (Period 07/93 - 03/94)", March 1994
- "Abschlußbericht (Period 04/94 - 09/94)", September 1994
- "Nachtrag zum Abschlußbericht (Period 10/94 - 12/94)", December 1994

JESSI AC-5 Reports:

- "Technical Report (Period 01/94 - 06/94)", July 1994
- "Technical Report (Period 07/94 - 12/94)", December 1994

JESSI AC-12 Reports:

- "Combined Milestone Report", January 1994
- "Technical Report (Period 01/94 - 06/94)", July 1994
- "Milestone Report", July 1994
- "Technical Report (Period 07/94 - 12/94)", December 1994
- "Combined Milestone Report", December 1994

OMSI Reports

- F. Buijs, E. Frank, T. Lengauer, 5. Halbjahresbericht (01.07.93 - 31.12.93), February '94
- F. Buijs, E. Frank, T. Lengauer, F. J. Rammig, 6. Halbjahresbericht (01.01.94 - 30.06.94), August '94

QUELLE Reports

- "1. Zwischenbericht (Period 08/93 - 05/94)", May 1994
- "2. Zwischenbericht (Period 06/64 - 08/94)", August 1994

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- "3. Zwischenbericht (Period 09/94 - 11/94)", November 1994

SYDIS Reports:

- E. Loeschner, J. Tacken, SYDIS-Zwischenbericht ueber das 2. Halbjahr 1993, Januar 1994
- E. Loeschner, J. Tacken, SYDIS-Zwischenbericht ueber das 1. Halbjahr 1994, Juli 1994
- J. Becker, F. Buijs, "Das SIR-Datenschema", August '94

JESSI-Common-Frame Reports:

- JCF/Cadlab/066-01/17-Feb-94 "Functional Specification of Hybrid Knowledge Representation and Access Component"
- JCF/CADLAB/067-01/March16,1994 "Problem Space Specification for HyKL Knowledge Access and Management Component"
- JCF/CADLAB/067-02/May 31,1994 "Problem Space Specification for HyKL Knowledge Evaluation Component"
- JCF/CADLAB/069-01/31-May-94 "HyKL 1.0 - Reference Manual"
- JCF/CADLAB/070-02/17-Aug-94 "User Requirements Specification for the HyKL Knowledge Access/Mangement and the Knowledge Evaluation Component"
- JCF/CADLAB/071-01/15-Aug-94 "Specification of the HyKL 1.0 Knowledge Evaluation Component"
- JCF/CADLAB/072-01/17-Aug-94 "Detailed Functional Specification for the HyKL Knowledge Access and Mangement Component"
- JCF/CADLAB/075-01/November 28,1994 "Detailed Functional Specification for the HyKL Knowledge Evaluation Component"

ASSET Reports:

- R. Böttger, Y. Engel, G. Kachel, S. Kolmschlag, D. Nolte, E. Radeke: "Asset-Report D.D3.4/1, Problem Analysis and Requirement Specification on Heterogeneous Database Systems", September 1994

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9 Collaboration in Technical-Scientific Bodies

GI, GME, ITG:

- Chairman of ITG Technical Committee 5.2 (CAD) (F.J. Rammig)
- Member of GI Technical Committee 3.5 (CAD) (F. J. Rammig, B. Steinmüller)
- Member of Steering Committee for Working Group GI 3.5.1/ITG 5.2.3 "Methods for the Design and Verification of Digital Circuits and Systems"(F. J. Rammig)
- Member of Steering Committee for Working Group GI 3.5.4/ITG 5.2.6 "CAD Umgebungen für den Entwurf mikroelektronischer Systeme" (B. Steinmüller, F. J. Rammig)
- VDI/VDE-GME Technical Committee "Informationstechnik für Mikrosysteme" (W. John)
- Member of VDE/ITG FG 5.2.2 "Hardwarebeschreibungssprachen und Modellierungsparadigmen", set up at EURO-VHDL '94 in Grenoble (W. Müller)
- Member of GI FG 4.2.1 AK 7 "Produktmodell / Datenmodellierung" (F. Buijs)
- Member of GI FG 2.5.1 "Datenbanken" (G. Kachel, E. Radeke)
- Member of Working Group "Petrinetze und Informationssysteme in der Praxis" (M. Brielmann, M. Niemeyer)

IFIP:

- National representative for Germany in IFIP TC10 (F. J. Rammig)
- Member of IFIP WG 10.5 (F. J. Rammig)

CFI:

- CFI Inter-Tool Communication Working Group (M. Joosten)
- CFI Working Group Simulation Backplane (M. Niemeyer)

Others:

- Member of Steering Committee of VHDL-Forum for Europe (F. J. Rammig)
- CFI TSC Component Information Representation European Co-chair (W. John)
- VHDL Reballoting Group (C. Oczko, W. Müller)
- Balloting Member of ANSI/IEEE Std 1076-1993, VHDL'93 (W. Müller)
- Contribution to the definition of EXPRESS Version 2 in the EXPRESS Working Group of DIN NAM 96.4.4 (W. Müller)
- Contribution to the definition of the SDAI in ISO TC184/SC4/WG7 "STEP Implementation Methods" (F. Buijs)

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- Balloting Member of IEEE Std 1164-1993 "IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164)" (W. Müller)
- IEEE Taskforce on the Engineering of Computer-based Systems, ECBS (M. Brielmann, F.-J. Stewing)
- Volunteer IEEE Technical Segment Committee on the Engineering of Complex Computer Systems, ECCS (F.-J. Stewing)
- Member of CENELEC TC117 WG1 (W. Müller)

Program Comittees, Organization of Sessions at Conferences:

- Topic Chair "Design Techniques and Methodologies", EDAC 94, Paris, France1994 (F. J. Rammig)
- Topic Chair "System Design with VHDL", EURO-VHDL 94, Grenoble, France 1994 (F. J. Rammig)
- Topic Chair "Design Issues for CAD Systems and Concurrent Engineering", EURO-DAC 94, Grenoble, France 1994 (F. J. Rammig)
- Program Chair IFIP International Conference EDAF 94, Gramado, Brazil 1994 (F. J. Rammig)
- PC Member CAD94 (Paderborn/Germany), VIUP94 (F. J. Rammig)
- PC Member IFIP International Conference EDAF 94, Gramado, Brazil 1994 (B. Steinmüller)
- PC Member GI/ITG-Workshop, FZI Karlsruhe, Germany 1994